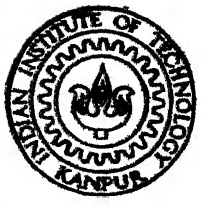
INVESTIGATION OF CARRIER TRANSPORT IN SURFACE BARRIER DEVICES ON POLYSILICON

By

K. M. PANCHAL



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INVESTIGATION OF CARRIER TRANSPORT IN SURFACE BARRIER DEVICES ON POLYSILICON

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K. M PANCHAL

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CERTIFICATE

This is to certify that the thesis entitled "Investigation of Carrier Transport in Surface Barrier Devices on Polysilicon" by K.M. Panchal is a record of work carried out under my supervision and has not been submitted elsewhere for a degree.

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August 7, 1980.

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Table of Contents

Notations

A	constant, $[V^{-1}]$
A^*	effective Richardson's constant, $[A/cm^2\ {}^oK^2]$
B	constant, $[K^{-1}]$
C	total device capacitance, $[F/cm^2]$
E_c	conduction band edge in silicon, [eV]
ΔE_F	Fermi level shift in grain boundary region, [eV]
E_{FB}	Fermi level in grain boundary region, [eV]
E_{FM}	Fermi level in metal, [eV]
E_{FS}	Fermi level in bulk silicon, [eV]
E_G	silicon bandgap, [eV]
E_o	defined by eqn. 2.5
E_{oo}	defined by eqn. 2.7
E_V	valence band edge in silicon, [eV]
F	fill factor
h	reduced Planck's constant, [Joule-sec]
I	device current, [A]
I_D	diode current, [A]
I_o	diode saturation current, [A]
J_D	diode current density, $[A/cm^2]$
J_o	diode saturation current density, $[A/cm^2]$
J_{RT}	recombination tunneling current density, $[A/cm^2]$
J_{sc}	short circuit current density of the cell, $[A/cm^2]$
J_{TT}	thermionic tunneling current density, $[A/cm^2]$
k	Boltzmann's constant, $[eV/{}^oK]$

m^*	effective mass of electrons in semiconductor, [kg]
n	diode ideality factor
N_{doping}	doping density, [cm^{-3}]
$N_{is}(E)$	interface state density, [$cm^{-2}\ V^{-1}$]
q	electronic charge, [C]
R_s	series resistance of the solar cell, [Ohm.cm^2]
T	absolute temperature, [^oK]
$T_{ox}(V)$	oxide tunneling transmission factor
V	device voltage, [V]
V_{oc}	open circuit voltage of solar cell, [V]
V_{ox}	oxide voltage, [V]
V_{ox}^o	oxide voltage at zero bias, [V]
w	width of grain boundary, [Å]
ϕ_B	Schottky barrier height, [V]
ϕ_B^*	barrier height obtained from activation energy plot, [V]
ϕ_B^n	Schottky barrier height for n-type silicon, [V]
ϕ_B^p	Schottky barrier height for p-type silicon, [V]
ϕ_{BG}	zero bias band bending at the grain boundary-bulk interface, [V]
ϕ_F	Fermi potential in bulk silicon, [V]
ϕ_M	metal work function, [eV]
ϕ_{MS}^*	$\phi_M - \chi_S$, [eV]
ϕ_n	$(E_c - E_{FS}) / q$ for n-type silicon, [V]

ϕ_p $(E_V - E_{FS})/q$ for p-type silicon, [V]

φ_1 interface potential in silicon, [V]

φ_1^0 interface potential in silicon at zero bias, [V]

ε_s silicon permittivity, [F/cm]

η conversion efficiency of solar cell

χ_s silicon electron affinity, [eV]

τ_T^{is} tunneling time for interface state carrier, [sec]

ABSTRACT

The present investigation has been mainly directed towards understanding the influence of grain boundaries, and other defects on carrier flow in surface barrier devices. With this in view, basically two types of studies had been carried out. One was related to investigation of carrier transport mechanisms in MOS diodes on polysilicon substrate. The other approach was to develop various techniques to characterize grain boundaries and to study their influence on electrical parameters of the device. These types of studies were useful for gaining better insight into the device operation on polysilicon material, particularly in view of the fact that MOS tunnel structures on polysilicon can be advantageously used as photovoltaic power converters.

MOS tunnel diodes were fabricated with gold as the barrier metal on Wacker n-type polysilicon, and with alminum as the barrier metal on Wacker p-type polysilicon. The diode current-voltage characteristics and capacitance-voltage characteristics of these devices were measured over a wide range of temperature, in order to identify the dominant transport mechanism. Plots of $\ln J_o$ vs $1/T$, $1/nT$, and T were obtained and a detailed analysis was carried out. Also, for better understanding of grain boundary influences on carrier flow, a comparative study was attempted by examining conduction mechanisms in MOS diodes on single crystal silicon

substrate. The results indicated that , depending upon the presence of traps in the silicon space charge layer and the magnitude of change in band bending with temperature in silicon, the dominant transport mechanism in these devices on polysilicon substrate could change from thermionic emission to thermionic field emission to multistep tunneling. It was also established that any hasty conclusions drawn without sufficient experimental data could lead to erroneous interpretetion of the dominant mechanism.

The electrical activities of grain boundaries were investigated in polysilicon material. For Wacker polysilicon, it was found that grain boundaries had a weak influence on electrical parameters of solar cell, and the collection efficiency of photogenerated carriers was not affected much in the vicinity of grain boundaries. Large grain boundary potential barriers were not observed in Wacker polysilicon, while an examination of Monsanto polysilicon gave some indication of existence of such barriers. The results on Wacker polysilicon were quite encouraging and gave promise for efficient solar cell performance when fabricated on this material.

1. INTRODUCTION

Recent interest in the investigation of carrier transport mechanisms in MOS tunnel diodes on polysilicon stems from their potential use in inexpensive large scale terrestrial application when used as solar cells. MOS tunnel diodes with the oxide thickness in the range 15-30 Å have been used profitably as MOS solar cells [1,2]. In these devices there can be a number of carrier transport mechanisms with a different one dominating over others in different temperature ranges. Even for a given device at a particular temperature, the same mechanism may not dominate over the entire bias regime [3-6]. In polycrystalline material, grain boundaries and other structural defects can also have varied influence on the carrier flow. It is important to investigate the carrier transport mechanisms as it controls the overall performance of the cell. The mechanism which reduces the diode current but leaves the light generated current undisturbed results in a larger value of open circuit voltage than others. Also, the diode ideality factor can have different values depending upon the conduction mechanism and influence the open circuit voltage and the fill factor of the cell. For understanding and improving the performance of MOS solar cells on polysilicon, an investigation of carrier transport mechanism in these type of devices coupled with the characterization of polysilicon material is essential. It is of considerable interest to review major developments in these directions.

As these type of studies are highly interrelated, a combined study would provide better insight of the influence of grain

boundaries on electrical parameters of the cell and resolve some of the basic questions regarding the device operation on polycrystalline material.

1.1 Carrier transport mechanisms in SB/MOS diodes

An important means of gaining physical insight into the current transport mechanisms in SB/MOS devices is to study the dark current-voltage and capacitance-voltage characteristics over a wide range of temperature. Considerable amount of work, theoretical as well as experimental, has been carried out in this direction and conduction phenomena of SB/MOS devices have been clarified to some extent. Wilson [7] tried to explain the rectifying action in SB diode in terms of quantum mechanical tunneling of electrons through a barrier, but it was soon realized that this mechanism predicted the wrong direction of current flow. However, Padovani et al. [8] and later Crowell et al.[9] presented theoretical and experimental results showing that the I_D-V characteristic of Schottky barrier formed on highly doped semiconductors can be interpreted in terms of the field and thermionic field emission over a wide temperature range. These were develo ments in carrier transport model for tunneling across the barrier.

The observed direction of rectification in metal-semiconductor diodes was explained by two distinct theories namely, Schottky's diffusion theory and Bethe's thermionic emission theory. Crowell and Sze [10] developed a theory in which both of these theories were incorported into a single thermionic emission diffusion theory as a generalized model for carrier transport.

Padovani et al.[11-13] and Saxena [14] investigated the current-voltage characteristics of Au-GaAs, Au-Si, Ni-Si, Cr-Si systems over a wide temperature range. They empirically found that the characteristics were dominated by a peculiar 'T_o' anomaly. 'T_o' was found to be a constant with the dimensions of temperature and independent of voltage and temperature over the temperature range studied. When 'T_o' was added to the absolute temperature 'T' in the exponential terms of the I_D-V characteristic, their experimental data was easily explained. In this case, diode ideality factor 'n' can be written as $n=1 + T_o/T$ and is temperature dependent. Padovani [15] also studied the reverse I_D-V characteristics of Au-GaAs Schottky barrier diode above room temperature and found that thermionic emission is a dominant mechanism for the reverse conduction, but his results could not be explained by the image force lowering theory.

Arizumi et al. [16] investigated transport properties of Schottky barriers on silicon surface with Ag, Au, Cu as barrier metals and reported temperature independent value of the diode ideality factor over the temperature range 100-350 ^oK with 'T_o' = 0. Until now no satisfactory explanation for the observed temperature anomalies has been given.

Saxena's [14] work provided a way to distinguish between the thermionic emission, thermionic field emission, and field emission mechanisms of carrier transport. However, when two or more conduction mechanisms are simultaneously responsible for the diode current, Saxena's procedure may not be adequate to identify the mechanism of carrier transport.

Most of the Schottky barrier diodes investigated had invariably an oxide thickness of 10 Å. Efforts have been made during the past few years in the direction of investigation of carrier transport mechanisms in MOS tunnel diodes with 20-40 Å thick oxide mainly because of their potential application in photovoltaics. The effect of oxide thickness on various mechanisms of carrier transport can be incorporated by means of an oxide transmission coefficient [6]. Kar [3,4,17] demonstrated possible mechanisms in these devices in his experimental investigation of the effect of oxide thickness and interface states on the diode current in MOS tunnel diodes. It was pointed out that thermionic emission-tunneling, recombination-tunneling via interface states and pure tunneling from accumulation layer could be the mechanisms which contribute to the diode forward current at room temperature.

Recently, Tarr and Pulfrey [18] have carried out measurements on Al-pSi MOS solar cells and reported the minority carrier injection as the dominating transport mechanism over the temperature range of 0-50 ^{o}C. This conclusion has been drawn mainly on the basis of the value of activation energy (1.19 $\pm$ 0.013 eV) from the activation energy plot. In this case, measurements of capacitance-voltage characteristics at different temperatures were not carried out to obtain information regarding the barrier height. Also, information regarding barrier height and interface states from independent sources such as small signal admittance and photoemission measurements is essential before drawing any firm conclusion on the basis of current-voltage characteristics only. Such type of conclusion can be erroneous.

transport mechanism in MOS tunnel diodes on polysilicon substrate. This is possibly due to the general belief that polysilicon may not produce reasonable solar cell efficiencies. Now that it is possible to achieve this, a systematic and detailed study is to be undertaken to understand the influence of grain boundaries on carrier flow. Kar et al. [5] have investigated carrier transport mechanisms in MOS diodes fabricated on p-type Wacker polysilicon with aluminum barrier metal, and in SOS diodes fabricated by chemical spraying of indium-tin oxide on n-type single crystal silicon. It has been pointed out that, at room temperature, multistep tunneling through the silicon barrier can be the dominant transport mechanism. In these devices, slopes of $\ln I_D$-V characteristics were found to be temperature independent and $\ln I_o$ vs.T plot was linear. Also, the diode current was weakly dependent on temperature. Such type of mechanism is possible in these devices in presence of a distribution of trap levels in the barrier region. In polysilicon material, grain boundaries present trap levels in the barrier region, while in SOS diodes traps may be introduced during chemical spraying or ion beam sputtering. Such type of tunnel-assisted transport process was detected before in case of p-n heterojunction [19,20], as well as in the case of ion beam sputtered ITO on p-type silicon SOS diodes [21]. It has been pointed out in the literature [22] that fluctuations in physical parameters over the diode area could cause ambiguities in the determination of the mechanism of current transport and this cannot be ruled out for the diodes on polysilicon substrate.

In addition to current-voltage and capacitance-voltage measurements at different temperatures to narrow down the probable conduction mechanisms, need arises to investigate the

these devices by seperate means. Such type of study would provide information about grain boundary potential barriers which may impede the carrier flow and determine the device characteristics.

1.2 Effects of grain boundaries in polysilicon solar cells

Grain boundaries are believed to be the most disastrous defect and plays a dominant role in determining the overall performance of the polysilicon solar cell. Various electrical activities of grain boundaries depend on a number of factors. Some of these factors can be the columnar or non-columnar nature of grain, whether a potential barrier exists at the grain boundary, and nature of the device configuration, i.e. whether pn or SB, etc.

In recent years some efforts have been made to characterize grain boundaries and to study their influence on the device performance.

Experimental work of Card et al. [23] and Seager et al.[24] invokes a model which proposes the presence of potential barriers located at the grain boundaries. These barriers affect the device characteristics in various ways depending upon whether the configuration is pn or surface barrier. The effect of potential barriers at the grain boundary, on the performance of MOS solar cells has been discussed in detail by S. Bhattacharya et al. [25] .

The influence of crystallographic defects and the defect-impurity complexes in p-n junction solar cells on Wacker polysilicon and EFG silicon ribbon has been studied by C.V. Hari Rao et al. [26]. The electrical activities of defects were

investigated in the scanning electron microscope operated in electron beam induced current (EBIC) mode. It was found that recombination processes in the vicinity of the grain boundary regions lead to a decrease in the electron beam induced current while twin boundaries were not found to be effective. Variation in collection efficiency of photogenerated carriers can be studied by using a photon beam scanner also. This method has an additional advantage over EBIC technique in that more detailed information can be obtained by using light sources of suitable wavelengths.

Fischer et al.[27] investigated the effect of grain size on the overall performance of the cell and pointed out the advantage of using Wacker cast polysilicon material with relatively large grain size (~150 um) and columnar structure. On this material they could achieve 10% AMI efficiency with p-n junction configuration. Studies on p-n junction solar cells indicate the possibility of achieving acceptable values of efficiency on polysilicon material. This shows some promise for low cost photovoltaic power generation but increased diffusion in the grain boundary region and the loss of photocarriers in the dead layer which becomes more serious in polycrystalline material sets them at a disadvantage.

Surface barrier devices have several advantages over the conventional p-n homojunction configuration such as inexpensive fabrication process, simple structure, and possibility of using less expensive material for fabrication. Low temperature processing involved in fabrication of these devices avoids degradation of minority carrier life time which is more important in polycrystalline material. Among various surface barrier configurations, the potential ability of MOS solar cells on single crystal silicon has been widely demonstrated in the past. If MOS cells on polysilicon provide

stability and acceptable value of efficiency, these cells on low cost polysilicon material will further bring down the cost of photovoltaic power generation.

MOS solar cell on Wacker cast polysilicon was first reported by Lillington and Tounsend [28]. On Al-pSi MOS with AR coating, they could obtain V_{oc} = 523 mV, J_{sc} = 22 mA/cm^2, F = 0.76 and η = 8.6% . This demonstrates that if design parameters of the cell are optimized, higher value of efficiency could be achieved. The performance of MOS solar cells on Wacker cast polysilicon has been also investigated by S. Bhattacharya et al. [29]. For MOS solar cells on n-type polysilicon with Ag barrier metal, V_{oc} = 515 mV, J_{sc} = 27.0 mA/cm^2, F = 0.71, η = 9.9% were obtained. For MOS solar cells on p-type polysilicon with Al barrier metal, V_{oc} = 467 mV, J_{sc} = 18.2 mA/cm^2, F = 0.69, η = 5.9% was obtained and no AR coating was used on these cells. The lower value of J_{sc} in case of Al barrier metal was due to higher reflection; but this can be increased with the help of AR coating. These results are encouraging. Also, it appears from the high value of fill factor that grain boundary shunting effects are negligible.

The results indicate that reasonable value of efficiency can be achieved on polysilicon surface barrier solar cells. However, in order to reduce or eliminate the unfavourable effects of grain boundaries and to realize a steady improvement in the performance of polysilicon solar cells, different techniques need to be developed to characterize grain boundaries.

1.3 Scope of the present work

The aim of the present work has been to study the carrier transport mechanisms in MOS tunnel devices on polysilicon and to investigate the influence of grain boundaries on the device performance. MOS tunnel diodes were fabricated for this purpose on Wacker cast polysilicon. Current-voltage and capacitance-voltage measurements at different temperatures in dark were carried out in order to investigate the carrier transport mechanisms in these devices. A comparative study was also attempted by examining the conduction mechanisms in the devices with identical fabrication conditions on single crystal silicon substrate to gain better understanding of grain boundary influences on the carrier flow in polysilicon material.

Various techniques were developed to characterize grain boundaries. An attempt was made to examine grain boundary potential barriers by measurements across grain boundaries. Room temperature studies on a number of dots on the solar cell arrays were taken up in order to investigate the influence of grain boundaries on the various electrical parameters of the cell. In this case, some of the dots were completely inside the grain, and others were over a varying number of perpendicular grain boundaries. The effects of grain boundaries on the light generated current were studied with a photon beam scanning arrangement. These types of studies would provide information about various electrical activities of grain boundary barriers and other defects in polysilicon material and lead to a better insight into the device operation.

2. THEORETICAL DISCUSSION

2.1 Carrier transport mechanisms in surface barrier diodes

2.1.1 Possible transport mechanisms

In case of surface barrier devices such as MOS and SOS diodes, there can be a number of carrier transport mechanisms which contribute to the diode current. In both MOS and SOS diodes, the potential barrier is formed at the silicon surface. In SOS diodes, the interface states at the oxide - degenerate semiconductor interface and located inside the degenerate semiconductor bandgap are localized while in MOS diodes states at metal - oxide interface are not localized. However, as far as the possible mechanisms of carrier transport in dark are concerned, the diodes hardly differ [5]. The energy band diagram of an MOS tunnel diode on p-type semiconductor under forward bias has been shown in Fig. 2.1. The possible carrier transport mechanisms are thermionic emission (process a), recombination tunneling via interface states (process b), thermionic field emission (process c), field emission (process d), multistep tunneling (process e), minority carrier injection (process f), and recombination in the space charge region (process g) [3-6].

2.1.2 Dependence of carrier transport mechanisms on device parameters

The forward current of an MOS tunnel diode is determined by a number of carrier transport processes (a-g). The relative magnitudes of these mechanisms depend upon various parameters, such as, barrier height, density of interface states, doping density of the semiconductor,

bias voltage, and temperature of the device [3,5]. An oxide layer of thickness < 35 Å is tunnelable to carriers. The effect of an oxide layer on the transport mechanisms can be taken into account by an oxide tunneling transmission coefficient [6]. The oxide tunneling transmission coefficient is not a constant but depends upon a number of parameters such as : oxide composition, $\phi_{MS}^{\ddagger}$, image force effect, device voltage, oxide thickness, and density of interface states. This has been discussed in detail elsewhere [1].

Generally in these devices, one observes that the forward current-voltage characteristics consist of three regions. The low bias regime is dominated by the recombination current (process g). This current is relatively more important at low temperatures and in materials with low life time. The high bias regime of the current-voltage characteristic is dominated by the series resistance effect. In the intermediate voltage regime, a number of processes (a-f) can dominate. The carrier transport mechanism in this bias regime is of more interest as it determines the overall performance of the solar cell. These processes are briefly discussed below.

Process a: In thermionic mode of carrier transport, the majority carriers overcome the silicon barrier by pure thermionic emission and there upon tunnel through the thin oxide layer. In this case, the total potential barrier can be treated seperately in terms of the silicon barrier and an oxide barrier. The resultant current density is determined by multiplying the thermionic current over the silicon barrier by a tunneling trranmission coefficient. The

expression for the thermionic-tunneling current density (J_{TT}) takes the form [17]:

$$J_{TT} = T_{ox}(V).\ J_O.\ \exp(qV/nkT) \qquad (2.1)$$

Where, $T_{ox}(V)$ is the oxide tunneling transmission coefficient, and n is the diode ideality factor. The expression for the diode saturation current density can be written as:

$$J_O = A^{**} T^2 \exp(-q\,\phi_B/kT). \qquad (2.2)$$

Process b: The transition of majority carriers from the silicon majority carrier band into interface states by recombination and then tunneling through the oxide into the metal causes an excess current. The recombination tunneling current assumes importance when either the interface state density is high, or the thermionic tunneling current is low because of high silicon barrier or low temperature, and at the lower values of the forward voltage [4,30,31]. Recombination-tunneling current density can be written as [3]:

$$J_{RT} = q \int_{E_{FM}}^{E_{FS}} N_{is}(E)\, dE/\tau_T^{is} \qquad (2,3)$$

Process C and Process d: Under certain circumstances, it may be possible for the majority carriers to penetrate the semiconductor barrier by direct tunneling. At sub-room temperatures, thermionic-field emission (process d) is the likely mechanism, and at low temperatures, field emission is the likely mechanism. The upper limit of temperature for these processes would extend further for

highly doped semiconductors. Except for very low value of forward bias, the J_D-V relationship for these mechanisms can be represented as [6]:

$$J_D = J_0 \exp (V/E_0) \tag{2.4}$$

where $E_0 = E_{00} \coth (q E_{00}/kT)$ for thermionic field emission, (2.5)

$$= E_{00} \quad \text{for field emission} \tag{2.6}$$

and $$E_{00} = \hbar/2 \, (N_{doping}/m^* \varepsilon_s)^{\frac{1}{2}} \tag{2.7}$$

In equation(2.4), J_0 is weakly dependent on bias, and is a complicated function of temperature, barrier height, and semiconductor parameters. Under simplifying conditions, this equation reduces to the form :

$$J_0 = A^* T^2 \exp (-q \phi_B/nkT), \tag{2.8}$$

for thermionic - field emission.

Process e: In presence of large number of traps in the silicon barrier region, multistep tunneling (process e) is a possibility. In this process, majority carriers tunnel by hopping via traps in the barrier layer. For such a mechanism, the diode current has been reported to be weakly dependent on temperature [19-21]. The forward current-voltage characteristic is expected to be of the form [19,20]:

$$J_D = J_0 \exp (AV) \exp (BT), \tag{2.9}$$

where A is a constant practically independent of voltage. In equation (2.9), ln J_0 is a linear function of temperature. Such type of mechanism has been observed by several investigators [5,19-21].

Process f: Minority carrier injection can be the controlling mechanism, if the barrier height is sufficiently large to suppress the majority carrier flow. For this mechanism, the current-voltage relationship can be written as:

$$J_D = J_0 \exp (qV/nkT), \tag{2.10}$$

where $J_0 \alpha T^3 \exp (-E_G/kT)$. (2.11)

2.1.3 Identification of dominant transport mechanisms

It can be seen from the above discussion that, the current-voltage characteristic of an MOS tunnel diode is the most difficult to interpret. Several mechanisms can occur in parallel and it is very difficult to seperate and identify a dominant mechanism contributing to the diode current in a particular diode. An effective means to narrow down the possible dominant mechanisms is to measure the current-voltage and high frequency capacitance-voltage characteristics of the device over a wide range of temperature. In addition information about interface state density can be obtained from small signal admittance-voltage characteristics in the forward bias regime. But this is possible only in thicker oxides.

From forward current-voltage characteristics at different temperatures, J_0 can be obtained at each temperature by extrapolation of the linear region of ln J_D-V characteristic to zero bias and plots of ln J_0 as a function of T,1/nT can be made. If thermionic emission of majority carriers over the top of the silicon barrier or minority carrier injection is to be the dominant transport mechanism, then

one obtains linear ln J_D -V characteristics over a wide range of temperature with a temperature independent diode ideality factor close to unity and a linear plot of ln J_0 against 1/T [5,6,14]. If at each temperature, the value of the barrier height obtained from the $1/C^2$-V plot is close to the value of the barrier height obtained from the activation energy plot, and if it is much different from the bandgap, then the thermionic emission is the most likely dominant mechanism. In this case, nT is expected to be a linear function of T [14]. However, seperation between thermionic emission and minority carrier injection becomes difficult if the value of the barrier height obtained from the activation energy plot is not much different from bandgap. One can also obtain a linear plot of ln J_0 against 1/T when recombination current dominates. But in this case, the value of the activation energy obtained is very much different from E_G and is close to $E_G/2$.

A linear ln J_D-V can also be obtained for thermionic field emission, field emission, or multistep tunneling mechanisms. If the diode current is temperature dependent, and if the plot of ln J_0 against 1/nT is linear, then thermionic field emission is the likely mechanism. In this case nT is expected to be a non linear function of T at low temperatures [14]. In case of field emission and multistep tunneling mechanisms, dependence of the diode current on temperature is negligible. For these mechanisms, the ln J_{D-V} plots at different temperatures have equal slopes, and ln J_0 varies linearly with T. The distinction between these two mechanisms becomes difficult at low temperatures. However,

at high temperatures, field emission is not probable and multistep tunneling can be expected to be the dominant mechanism.

The idea of taking current-voltage and capacitance-voltage characteristics over a temperature range 77-400 ^{o}K often exists in literature, to identify the transport mechanisms. However, the same mechanism may not dominate over the entire temperature range, and there can be different transport mechanisms in different temperature ranges. This has been reported recently by S. Ashok et al [32].

2.2 Grain boundary studies

2.2.1 Transport across grain boundaries

Polycrystalline silicon consists of a large number of randomly oriented grains of different size and shape which are seperated by grain boundaries. Apart from physical discontinuties arising from grain boundaries, other defects such as dislocations, stacking faults, and impurities can also be present. These defects can have varied influence on the carrier flow. Recent reports on the measurements of the resistivity of polysilicon proposes the presence of potential barriers at grain boundaries [23,24]. Grain boundary potential barriers are formed in semiconductors because the chemical potential in the grain boundary region is shifted from the bulk value due to the lack of perfect periodicity. Also, depending upon the method of preparation, the grain boundary regions may contain a large number of point defects, impurities or other phases. This also can result in a shift of the chemical potential.

If the grain boundary region has a lower chemical

potential for majority carriers than the bulk, then the resultant influx of majority carriers to the boundary would necessarily lead to the formation of a depletion region in order for charge neutrality to be maintained and thus creating a potential barrier. This barrier will impede normal transport of majority carriers. However, it is quite possible that the opposite shift of the grain boundary chemical potential can occur, i.e., the grain boundary region has a higher chemical potential than the bulk. In this, case, the resultant space charge layer is an accumulation region which has negligible influence on majority carrier transport.

The energy band diagram of the region of an n-type semiconductor, describing two semi-infinite grains and one grain boundary, before and after joining has been shown in Fig. 2.2 (a) and Fig. 2.2 (b) respectively. It has been assumed that the chemical potential in the grain boundary region has a lower value than the bulk of the semiconductor grains. In equilibrium, the accumulated charge near x=0 causes the energy bands to bend upwards by an amount ΔE_F. It has been proposed that the majority carriers overcome the barrier by thermionic emission [34,36]. In this case, minority carriers which arrive at the barrier edge will be transported quickly to the grain boundary. Additional barriers can be introduced to the carrier flow because of large perturbations of the bandgap caused by local distortions or the presence of substantial amount of second phase at the grain boundary. These barriers would cause the grain boundary transport properties to differ considerably from the simple model discussed above.

2.2.2 Effect of grain boundaries on electrical characteristics

The influence of grain boundaries on electrical parameters of the solar cell will depend upon the nature of grain boundaries. Transverse grain boundaries, which intersect the current axis of the cell, can cause a catastrophic loss in the collection of the optically generated carriers. The loss of photocarriers decreases with the grain boundary making a smaller angle with the current axis. The grain boundary will have the least effect upon the collection of photo carriers when it lies parallel to the current axis. The influence of such grain boundaries as recombination sites will be very small. Hence, the columnar nature of the individual grain is always preferred to generate acceptably efficient solar cell performance on polycrystalline substrate. The columnar grains can affect the device characteristics in various ways depending upon a number of factors. These are whether the junction is pn or a surface barrier, whether a potential barrier exists at the grain boundary, and whether the conduction along the boundary is easy or difficult. In surface barrier configuration of the solar cell, the diode current is due to the transport of majority carriers, while the light generated current is due to the transport of minority carriers. In this case, the existence of potential barriers will affect the diode and light generated current in a different manner. Suppose that the potential barrier formed is in such a way as to attract minority carriers towards the grain boundary but repel majority carriers. In this case, the diode current should not be affected unless the material contains a large number of grain boundaries. Now, if the

conduction along the grain boundary is easy then, the short circuit current may not be altered much in the presence of grain boundary. However, it will get reduced if the conduction along the boundary is difficult.

Now, suppose that the potential barrier formed is in such a way as to attract majority carriers but repel minority carriers. In this case, the short circuit current density may not be altered much. Now, if the conduction along the grain boundary is easy, then the diode current will increase. This will result in a lower value of open circuit voltage and the fill factor and will degrade the device performance. On the other hand, if the conduction along the grain boundary is difficult, the diode current may not be affected or can even get reduced. This would lead to higher value of open circuit voltage [25]. It can be seen that the surface barrier solar cells are expected to perform better on polycrystalline substrate. In pn junction solar cells, the diode current and the light generated current are influenced in the same manner by the situation in the grain boundary region. This would set them at a disadvantage.

It has been reported that grain boundary potential barriers may not exist under illumination [37]. However, the grain boundaries continue to act as recombination sites and are responsible for the photovoltaic properties of polysilicon solar cells. Recent experiments of Seager et al. [33,38] indicate that preferential diffusion of certain foreign chemical species into the grain boundaries would promote significant changes in the density of defect states in the grain boundary regions. This can be used to advantage in case of surface barrier solar cells.

3. EXPERIMENTAL PROCEDURE

3.1 Device fabrication

The essential steps involved in the fabrication of MOS tunnel devices on single crystal silicon and polysilicon are surface cleaning, growing a thin interfacial oxide layer, evaporation of the barrier metal at the front followed by evaporation of the back ohmic contact. In case of the device fabrication on polysilicon to study grain boundary potential barriers, the steps involved are surface cleaning and evaporation of ohmic contact metal on the front surface. The fabrication sequence of these devices is shown in Fig. 3.1. All the fabrication steps were carried out in clean room environment.

3.1.1 Surface cleaning

Surface cleaning is the starting and critical process in the fabrication sequence and was carried out on single crystal and polysilicon wafers. P-type single crystal wafers (111) of 0.1-1.0 Ohm.cm. resistivity had polished front and lapped back surface. N-type polysilicon wafers of 1.0-10.0 Ohm.cm. resistivity and p-type polysilicon wafers of 1.0-10.0 Ohm.cm. resistivity were obtained from Wacker Chemitronic. Monsanto p type polysilicon wafers of 0.1-0.3 Ohm.cm. resistivity were also used for making devices. The grains were of different shapes and dimensions varied between 1 and 8 mm. Surface cleaning included degreasing with organic solvents followed by chemical etching with acids. The wafers were cleaned in a clean chemical bench, and all solvents and acids used were of electronic grade. Chemical etching was found to be the most critical step for the removal of damaged layer from the surface of polysilicon. For

polycrystalline material, steps followed in sequence were as follows.

(i) The wafer was degreased by treating in warm trichloroethylene for about 2 minutes and then in warm acetone for 2 minutes to remove traces of trichloroethylene followed by warming in methanol for removing traces of acetone.

(ii) The wafer was then chemically polished by etching in a mixture of CP4 and HNO_3 (1:1) for 2 minutes to remove the damaged surface layer from either side.

(iii) The wafer was rinsed in deionized water several times to remove traces of acids.

For Monsanto wafer, chemical polishing resulted in unsmooth wafer surface and step (ii) was replaced by etching in HF to remove any oxide layer present on the wafer surface.

The cleaning of single crystal silicon involved step (i) as mentioned above followed by the steps below.

(ii) The wafer was etched in HF to remove the intrinsic oxide.

(iii) The wafer was rinsed in deionized water several times to remove traces of HF.

(iv) This was followed by treating the wafer in warm HNO_3 for about 5 minutes to grow an oxide about 50-60 A^{o} thick.

(v) The wafer was rinsed in deionized water several times to remove traces of HNO_3.

(vi) The wafer was etched in HF again to remove freshly grown oxide.

(vii) Finally, the wafer was rinsed several times in deionized water to remove traces of HF.

Steps (iii) (v) were necessary to avoid chemical etching of the surface which would damage the flatness of the surface.

After this surface cleaning process, the wafer surface came out hydrophobic and was ready for further processing.

3.1.2 Oxidation

Immediately after chemical cleaning of the wafer, a thin interfacial layer of oxide was grown at a high temperature in dry oxygen. The oxidation was carried out in a horizontal flow, open end 60 mm i.d. fused silica tube in a three zone Thermco Spartan furnace. Dry oxygen was bubbled through a liquid nitrogen trap before admitting into the furnace tube. After loading, the wafer was kept at the mouth of the tube for a short time to dry the wafer surface completely before moving into the hot zone. The oxide was grown at a temperature of 700 ^{o}C and at an oxygen pressure of 1.0 atmosphere for 60 seconds. The oxygen flow rate was more than 1.0 litre/min. For these oxidation conditions, the thickness of the oxide layer was found to be 20 Å [3c]. The oxide of this thickness is tunnelable to carriers and has been reported to be optimum for the solar cell performance [1,2].

3.1.3 Metallization

The metallization was carried out in an oil free high vacuum system (Grainville Phillips Co. USA, series 252) having a digital quartz crystal thickness monitor (Perkin Elmer, USA, Model 605-1210). To minimize oil contamination liquid nitrogen traps were used with rotary and diffusion pumps.

For evaporation of aluminum and gold, tungsten helical filament was used. A tungsten conical basket was used for silver evaporation. The metals evaporated were obtained in form of wires, 1.0 to 1.5 mm in diameter and had 5N purity. The tungsten filaments were thoroughly degreased in warm trichloroethylene, acetone, and methanol, and were then outgassed in

vacuum by passing higher current than that required for evaporation of metals. The metals were degreased in the same procedure used for filaments and degassed before an evaporation. At the time of degassing, a shutter was kept between the source and the substrate in order to prevent contamination of the substrate surface by any foreign volatile species coming out. To ensure a uniform film and to reduce substrate heating, the source to substrate distance was kept more than 10 cm.

On n-type silicon Au, Ag were used as barrier metals and Al was used for the ohmic contact. On p-type silicon, Al was used as barrier metal and Au, Al were used as ohmic contact metals. The choice of barrier metals and ohmic contact metals have been discussed in detail elsewhere [1].

MOS tunnel diodes with thick metal layer were fabricated on polysilicon as well as on single crystal silicon in order to study carrier transport mechanism. Thick circular dots of 0.4 and 0.5 mm diameter of the barrier metal were deposited through molybdenum masks on the front surface. This was followed by deposition of ohmic contact metal on the back surface. The rate of deposition for the back contact and thick dot was kept above 10.0 Å /sec.

Thin metal layer deposition was carried out on polysilicon for studying the photovoltaic behaviour of MOS tunnel diodes with polysilicon as substrate and arrays contained some dots inside the grain and others located over varying number of grain boundaries. Metal layer thickness was in the range of 50 to 120 Å and the deposition rate between 1.0 and 6.0 Å/sec. Also, large area solar cells with diameter 5 to 7 mm

were fabricated on polysilicon and were used in the photon beam scanning analysis.

Arrays consisting of 0.4 and 0.5 mm diameter dots were also made on polysilicon to study grain boundary barriers. Thick circular dots of Al were evaporated through molybdenum masks on one surface of the n-type wafer and an Al strip about 1 mm in width was evaporated near the edge of the wafer. Au was evaporated similarly on p-type polysilicon. The choice of the metal was dictated by the fact that this should form ohmic contact on polysilicon, for any barrier formation would otherwise obscure the effects of grain boundary potential barrier.

The chamber pressure was kept well below 1.0×10^{-5} torr during all evaporations.

3.2. Measurements

3.2.1 Measurements at different temperatures

A simple heating arrangement consisting of two polished brass discs with a heating element wound on a mica sheet in between was employed. This was fitted closely in a hollowed out teflon block. The device was mounted in a shielded, light tight box, on a gold plated brass disc, which formed one contact terminal. The temperature of the disc was accurately measured with the help of a chromel-alumel thermocouple and a Leeds and Northrup type 8691 millivolt potentiometer. The temperature of the disc was controlled precisely within $\pm$ 0.5 ^{o}C by a temperature controller. The front contact on the device was made with the help of a telescopic spring probe with a very sharp tip. Care was taken to prevent any lateral movement of the block after the front contact was made. The

current-voltage and capacitance-voltage measurements were carried out in dark at various values of temperatures.

3.2.1.1 Current-Voltage Measurements

The circuit diagram used for the measurement of diode current at different values of bias is shown is Fig. 3.2 (a). Measurements were carried out in dark. The diode current as a function of applied bias was plotted on a semilogarithmic graph. The diode ideality factor n was obtained from the slope of the linear region of the forward ln I_D-V characteristic using the relation $n=(q/kT)\ (dV/d\ \ln I_D)$. The reverse saturation current I_0 was obtained by extrapolating the linear region of the forward ln I_D-V plot to zero bias. This was used to determine the barrier height. The series resistance was obtained from the linear range of the I_D-V characteristic.

3.2.1.2 Capacitance-Voltage Measurements

The capacitance-voltage characteristics were measured at 100 kHz using the set up shown in Fig. 3.2 (b). The a.c. signal voltage of the capacitance bridge was kept below 15 mV peak-to-peak to avoid any inaccuracy due to the non linear charge-voltage relation of the device.

The device capacitance was measured at regular bias intervals up to considerably large reverse bias values. The plot of reciprocal of the squared capacitance as a function of bias was a straight line. The doping density and the zero bias silicon band bending were obtained from the slope of the straight line and the intercept on the bias axis, respectively, by using the relations [1,40]:

$$N_{doping} = 2/(q.\varepsilon_s.\ln(1/C^2)/dV), \quad (3.1)$$

$$\varphi_1^o = V_{intercept} - (kT/q) \text{ for n-type}, \quad (3.2a)$$

$$\varphi_1^o = -V_{intercept} + (kT/q) \text{ for p-type} \quad (3.2b)$$

The zero bias barrier height was obtained according to the relations:

$$\phi_B^n = \varphi_1^o + \phi_n, \quad (3.3a)$$

$$\phi_B^p = \varphi_1^o + \phi_p. \quad (3.3b)$$

3.2.2 Studies on grain boundary effects

Various techniques were developed for characterizing grain boundaries.

To study the effect of grain boundaries on the electrical parameters of the solar cell on polysilicon, current-voltage and capacitance-voltage measurements were carried out at room temperature in dark on number of dots in the cell array. Measurements were made on the dots located over a single grain and a varying number of grain boundaries. The device was mounted in a shielded, light tight box, on a water cooled copper block which formed one contact terminal. The other contact was made to the dots with the help of a very sharp tip telescopic probe. During measurements under illumination, the box cover was uncovered. The procedure for current-voltage and capacitance-voltage measurements has been discussed in 3.2.1.1 and 3.2.1.2, respectively. For the same dots, the values of open circuit voltage and short circuit current density under AMI

illumination was also observed. AMI illumination was simulated with the help of a 150 W tungsten lamp and checked with the help of a commercial OCLI p-n junction solar cell.

A photon beam scanning arrangement was set up to study the effect of grain boundaries and other imperfections on the light generated current of the solar cells on polysilicon. Optics of this arrangement is shown in Fig. 3.3. This consisted essentially of an arrangement to focus the light coming from a collimated source to a very fine beam of less than 0.5 mm in diameter. The focussed beam was made to fall over the solar cell mounted on a gold plated copper block, stationed on the micropositioner platform of the microscope with X-Y movement capability enabling one to move the device in the X or Y direction relative to a stationary light beam. Two spring probe attachment was provided to make contact on the sample. The photon-beam-induced current was measured as the sample was scanned by a light beam. The grain structure of the device was viewed through a microscope.

Grain boundary potential barriers were examined by measuring the current-voltage characteristics across the grain boundary. The arrangement for mounting the device and making contact was the same as described above. Contacts were made on the strip and the dot or between two dots so that only one grain boundary was incorporated between them. Measurements of current-voltage characteristics were carried out in dark and ploted on a linear graph. Next, two or more grain boundaries were incorporated between the contacts and the same measurements were repeated.

4. RESULTS AND DISCUSSIONS

4.1 Studies of carrier transport mechanisms

4.1.1 MOS diodes on single crystal silicon

MOS diodes with aluminum as the barrier metal were fabricated on p-type single crystal silicon wafers with bulk resistivity of 0.1 to 1.0 Ohm. cm. The oxide thickness was about 20 Å. The back ohmic contact was gold for all these devices. Forward current-voltage characteristics of these devices were measured in dark at different temperatures spanning the range: 294 to 414 °K. Corresponding high-frequency measurements were also carried out in dark. Temperature of the device was controlled accurately with a temperature controller, and the maximum error involved in temperature measurements was ± 0.5 °C. The measured current voltage characteristics at different temperatures have been presented in Fig. 4.1. Corresponding C^{-2}-V characteristics are shown in Fig. 4.4. The important experimental data obtained from these measurements have been listed in Table 4.1 for a representative device. The doping density, calculated from the slope of C^{-2}-V characteristics correspond to the bulk resistivity data obtained on this material. The bulk Fermi level ϕ_F was calculated from the experimentally obtained doping density. The device area was measured under a microscope.

It can be seen from Table 4.1 that with increasing temperature, the zero bias band bending φ_1^o decreases and the value of bulk Fermi potential ϕ_F increases. According to the energy band diagram given in Fig. 2.1,

$$\varphi_1^o = (E_G + \chi_s - \phi_M)/q - V_{ox}^o - \phi_F.$$

A part of change in φ_1^o with temperature can be accounted by the change in the bandgap E_G and the bulk Fermi level ϕ_F. It is also expected that the work function of the metal and the electron affinity of silicon would change with temperature, although there does not seem to be any experimental data to support this [6]. It may be noted that, over the entire temperature range the total change in zero bias silicon bandbending, $\Delta\varphi_1^o$, is 0.12V, whereas $(E_G/q - \phi_F)$ is 0.10 V, cf., Table 4.1. Hence, $\Delta\varphi_1$ can be, more or less explained by the change in the bandgap and the bulk Fermi level with temperature. Attempts can be made to relate the change in the interface state charge with the change in the Fermi level position. But, this would lead to contradiction of the experimental results. Experimentally, $(\varphi_1^o + \phi_F)$ has been found to decrease with temperature (cf., Table 4.1). This would mean that the Fermi level at higher temperature will be farther away from the conduction band edge at the $Si-SiO_x$ interface. The result is that the interface state charge becomes less negative due to a change in occupancy of the interface states. This would cause a decrease in the oxide potential V_{ox}^o which should lead to an increase in $(\varphi_i^o + \phi_F)$. This is in contradiction with the observed behaviour of $(\varphi_i^o + \phi_F)$ with temperature. The $\ln I_D$-V characteristics of the device exhibit fairly good exponential behaviour over 2-3 decades of current,

cf., Fig. 4.1. Recombination and interface recombination-tunneling components seem to be negligible. The diode ideality factor n has been obtained from the slope of the linear region of the $\ln I_D$-V characteristic. The value of n is more or less constant except for the highest temperature, 414 ^{o}K. The extrapolation of the linear region of the $\ln I_D$-V characteristics to zero bias gives the reverse saturation current at each temperature . The corresponding current densities listed in Table 4.1 have been used to obtain activation energy plots of $\ln J_o$ vs 1/T and 1/nT. These plots have been presented in Fig. 4.2. It can be seem that both plots are equally linear. However, the value of the barrier height obtained from the $\ln J_o$ vs 1/nT plot comes out to be 1.08 V, whereas the value obtained from $\ln J_o$ vs 1/T plot is 0.76 V. It can be seen that the value of the barrier height obtained from the $\ln J_o$ vs 1/nT plot is more close to the value of $(\varphi_i^o + \phi_F)$, cf., Table 4.1. The relation for thermionic emission can also be used to calculate the value of the barrier height ϕ_B from the intercept of the linear region of the forward $\ln I_D$-V characteristic, assuming that the carrier transmission coefficient through the oxide is unity. However, it may be observed from Table 4.1 that while $(\varphi_i^o + \phi_F)$ decreases with temperature, ϕ_B increases. Fig. 4.17 contains plot of nkT/q vs kT/q and it is evident from the nature of the plot that thermionic emission is the likely mechanism [14]. The variation of $\ln J_o$ vs T has been presented in Fig. 4.3. The non linear relationship observed between $\ln J_o$ and T

indicates that the field emission is not the probable mechanism of carrier transport in this device.

4.1.2 MOS diodes on polysilicon

4.1.2.1 MOS diodes on p-type polysilicon

The measured forward current-voltage characteristics of a typical MOS device Al 25 P C3 on p-type polysilicon, are presented in Fig. 4.5. Corresponding $1/C^2$-V characteristics are shown in Fig. 4.8. Measurements were taken for the device temperatures of 294, 314, 334, 354, 374, 394, and 414 ^{o}K. The diode had gold as the back ohmic contact. The interfacial layer thickness was about 20 Å. The results of measurements on this device have been summarized in Table 4.2. The behaviour of φ_1^o, ϕ_F, and $(\varphi_1^o + \phi_F)$ with temperature is similar to what has been observed in the case of MOS diodes on p-type single crystal silicon. In this case, the total change in zero bias band bending between 294 and 394 ^{o}K is 0.23 V, whereas $(E_G/q-\phi_F)$ is 0.10 V, cf., Table 4.2. It can be seen that the total change in φ_1^o can only
/be partially accounted by the corresponding change in E_G and ϕ_F. Also, as has been discussed in sec. 4.1.1, the behaviour of φ_i^o with temperature cannot be explained by change in the interface states occupancy due to the shift in the bulk Fermilevel. The $\ln I_D$-V characteristics of Fig. 4.5 indicate an exponential behaviour over 2-3 decades. The value of the diode ideality factor n is found to be constant except for the highest temperature at which the device characteristic might have undergone

a change due to constant heating. In Fig. 4.6, $\ln J_o$ has been plotted as a function of 1/T and 1/nT. It can be seen that the plot of $\ln J_o$ vs 1/nT is linear, whereas the plot of $\ln J_o$ vs 1/T deviates from linearity. The value of the barrier height obtained from $\ln J_o$ vs 1/nT plot comes out to be 1.04 V, which is close to the value of $(\varphi_i^o + \phi_F)$, cf., Table 4.2. For this device, the plot of $\ln J_o$ vs T is linear. This is some indication of the presence of a tunneling component contributing to the diode current. However, from Fig. 4.17, it can be seen that the plot of nkT/q vs kT/q is linear. This indicates that pure tunneling is not the dominant transport mechanism [14].

It should be noted that, in presence of a tunneling component, the value of barrier height ϕ_B, obtained(cf., Table 4.2) from Eq. 2.2 by assuming thermionic emission as the dominant mechanism, may not represent the true value.

4.1.2.2 MOS diodes on n-type polysilicon

Studies have been conducted on Au n-Si MOS diodes on polysilicon substrate and the experimentally observed values of various parameters of two typical diodes have been summarised in Tables 4.3 and 4.4. These devices had an interfacial layer thickness of about 20 Å and the back ohmic contact was aluminum.

Figures 4.9 and 4.12 represent the $\ln I_D$-V and $1/C^2$-V characteristics, respectively, of device Au 76 P B3 at device temperatures of 298, 316, 336, 357, 376, 396, and 415 ^oK. In Figs. 4.13 and 4.16 are presented the $\ln I_D$-V and $1/C^2$-V characteristics, respectively, of device Au 56 P B5 at device temperatures of 307, 327, 345, 365, 385,

Table 4.3 contains the important experimental data for the device Au 76 P B3. The variation of φ_1^o, ϕ_F, and $(\varphi_1^o + \phi_F)$ with temperature follows similar trend as observed for MOS diodes. Since $\varphi_1^o = (\phi_M - \chi_S)/q - V_{ox}^o - \phi_F$ for n-type semiconductor, a part of change in φ_1^o with temperature can be explained as due to a corresponding change in the bulk Fermi level ϕ_F. However, this does not completely account for the total change in φ_1^o, i.e. $\Delta\varphi_1^o = 0.16$ V, whereas $-\phi_F$ is only 0.09 V, cf., Table 4.3.

For this device, the general features of the $\ln I_D$-V characteristics and the nature of $\ln J_o$ vs T^{-1}, $1/nT$, and T plots, are similar to those of device Al 25 P C3. The diode ideality factor is found to be temperature independent.

Table 4.4 lists the data obtained from $\ln I_D$-V and $1/C^2$-V characteristics on device Au 56 P B5. For this device, $\Delta\varphi_1^o = 0.28$ V, in the temperature range 307 to 425 ^oK. This change is very large and can not be accounted by the shift in the Fermi level with temperature.

The $\ln I_D$-V characteristics presented in Fig. 4.13 do not follow the trend as has been observed in case of devices Al 1 B2, Al 25 P C3, and Au 76 P B3. An unusual feature of these characteristics is that the slope is temperature independent. Thermionic emission of majority carriers over the silicon barrier or minority carrier injection is not the probable transport mechanism because of the following reasons. First, the diode ideality factor is much higher than 1.0 and depends strongly on temperature.

Second, a plot of $\ln J_o$ vs T^{-1} has been found to be strongly non-linear, indicating that an activation energy is not involved in the dominant mechanism of carrier transport. Also, for minority carrier injection, much smaller values of J_o can be expected for moderately doped semiconductors. Thermionic field emission is also ruled out, because nT is independent of temperature and $\ln J_o$ vs $1/nT$ is a vertical plot [14]. This leaves field emission through the silicon barrier as the possible transport mechanism. This conclusion can be arrived at because of the fact that, $\ln J_o$ vs T plot is linear, and nT is independent of temperature [14,15]. However, for moderately doped semiconductors, and at high device temperatures, field emission is not the probable mechanism [6]. This type of behaviour has been observed by several workers [5,19-21]. It has been suggested that, in presence of large number of traps in silicon barrier region, multistep tunneling is a probable mechanism. If this mechanism is assumed to be dominant, then from Eq.2.9, the values of A and B come out to be 18 V^{-1} and 0.04 K^{-1}, respectively. In comparision, for Al p-Si MOS diodes on polysilicon, the value of A obtained was 22 V^{-1} and that of B was 0.052 K^{-1} [5]. For SOS diodes fabricated by chemical spraying of ITO on n-type silicon, the value of A obtained was 23 V^{-1} and that of B was 0.05 K^{-1} [5]. This indicates that, the values of A and B obtained for device Au 56 P B5 do confirm to the reported values. For

multistep tunneling process, σ_1^o is responsible for the change in I_D with temperature [21]. It can be seen that $\Delta\varphi_1^o$ between 307 to 425 ^oK is 0.28 V, cf., Table 4.4, whereas the corresponding voltage displacement in the $\ln I_D$-V characteristics is 0.26 V, cf., Fig. 4.13. Hence the change in I_D with temperature can be explained by $\Delta\varphi_1^o$. The existance of a large number of trap levels in polysilicon can arise due to the presence of grain boundaries, dislocations and other defects.

Table 4.1: Experimentally obtained values of various parameters of an MOS device A1 1 B2

T (^{o}K)	φ_i^o (V)	N_{doping} (cm^{-3})	Φ_F (V)	$\varphi_1^o + \Phi_F$ (V)	J_o (A cm^{-2})	n	nT (^{o}K)	Φ_B (V)	Φ_B^x (V)
294	0.96	2.16×10^{16}	0.16	1.12	2.1×10^{-9}	1.33	391	0.91	
313	0.94	2.22×10^{16}	0.17	1.11	2.1×10^{-8}	1.34	419	0.91	
334	0.92	2.22×10^{16}	0.18	1.10	1.2×10^{-7}	1.33	444	0.93	1.08
354	0.90	2.28×10^{16}	0.19	0.09	6.6×10^{-7}	1.33	470	0.94	
374	0.88	2.28×10^{16}	0.20	1.08	2.4×10^{-6}	1.32	494	0.95	
394	0.86	2.31×10^{16}	0.21	1.07	8.4×10^{-6}	1.31	576	0.96	
414	0.84	2.31×10^{16}	0.22	1.06	2.4×10^{-5}	1.28	530	0.98	

The area of this device was 1.2×10^{-3} cm^2.

Table 4.2: Experimentally obtained values of various parameters of nMOS device Al 25 P C3.

T (^{o}K)	φ_i^o (V)	N_{doping} (cm^{-3})	Φ_F (V)	$\varphi_i^o + \Phi_F$ (V)	J_o (A cm^{-2})	n	nT (^{o}K)	Φ_B (V)	Φ_B^* (V)
294	0.80	6.27×10^{15}	0.19	0.99	9.8×10^{-9}	1.29	379	0.87	
314	0.76	6.42×10^{15}	0.20	0.96	6.7×10^{-8}	1.29	404	0.89	
334	0.72	6.42×10^{15}	0.21	0.93	3.8×10^{-7}	1.29	430	0.90	1.04
354	0.66	6.42×10^{15}	0.22	0.88	2.0×10^{-6}	1.29	455	0.90	
374	0.62	6.47×10^{15}	0.24	0.86	1.1×10^{-5}	1.28	480	0.90	
394	0.57	6.47×10^{15}	0.25	0.82	4.3×10^{-5}	1.28	506	0.91	
414	0.54	6.52×10^{15}	0.26	0.80	7.4×10^{-4}	1.60	662	0.86	

The area of this device was 1.2×10^{-3} cm^2.

Table 4.3: Experimentally obtained values of various parameters of an MOS device Au 76 P B2.

T (^{o}K)	φ_i^o (V)	N_{doping} (cm^{-3})	Φ_F (V)	$\varphi_1^o + \Phi_F$ (V)	J_o (A cm^{-2})	n	nT (^{o}K)	Φ_B (V)	Φ_B^* (V)
298	0.60	2.94×10^{15}	0.23	0.83	2.7×10^{-7}	1.32	393	0.81	
316	0.57	3.46×10^{15}	0.25	0.82	4.6×10^{-7}	1.31	414	0.84	
336	0.54	3.59×10^{15}	0.26	0.80	2.4×10^{-6}	1.31	440	0.85	0.90
357	0.51	3.73×10^{15}	0.28	0.79	1.0×10^{-5}	1.31	468	0.86	
376	0.48	4.04×10^{15}	0.30	0.78	4.1×10^{-5}	1.31	493	0.87	
396	0.46	4.41×10^{15}	0.31	0.77	1.4×10^{-4}	1.31	519	0.87	
415	0.44	5.11×10^{15}	0.32	0.76	4.8×10^{-4}	1.32	548	0.87	

The area of this device was 7.9×10^{-3} cm^2.

Table 4.4: Experimentally obtained values of various parameters of an MOS device Au 56 P B5

T (^{o}K)	φ_i^o (V)	N_{doping} (cm^{-3})	Φ_F (V)	$\varphi_1^o + \Phi_F$ (V)	J_o (A cm^{-2})	n	nT (^{o}K)	Φ_B (V)
307	0.66	1.96×10^{15}	0.25	0.91	5.6×10^{-6}	2.14	657	0.75
327	0.60	2.12×10^{15}	0.27	0.87	1.1×10^{-5}	2.01	657	0.78
345	0.54	2.32×10^{15}	0.29	0.83	2.2×10^{-5}	1.90	656	0.81
365	0.50	2.63×10^{15}	0.30	0.80	5.1×10^{-5}	1.80	657	0.83
385	0.42	2.83×10^{15}	0.32	0.74	1.0×10^{-4}	1.71	658	0.86
405	0.41	3.82×10^{15}	0.32	0.73	2.4×10^{-4}	1.62	656	0.88
425	0.38	4.78×10^{15}	0.34	0.72	5.3×10^{-4}	1.54	655	0.89

The area of this device was 1.3×10^{-3} cm^2.

4.2 Grain boundary studies

4.2.1 Transport across grain boundaries

Studies have been carried out to investigate grain boundary potential barriers in Wacker polysilicon and Monsanto polysilicon material. The bulk resistivity of Wacker p-type and n-type polysilicon wafers was 1.0-10.0 Ohm. cm., while for Monsanto p-type it was 0.1-0.3 Ohm. cm. Figs. 4.18 and 4.19 display current-voltage characteristics for typical devices fabricated on Wacker n-type and p-type polysilicon, respectively. The ohmic contact metal was gold for p-type polysilicon and aluminum for n-type polysilicon. The I-V measurements were carried out by incorporating different number of grain boundaries between contacts. These characteristics show essentially an ohmic behaviour regardless of the number of grain boundaries inbetween contacts. The resistance involved is of the order of 100 Ohms which can nearly be accounted for by the bulk resistivity of the material. This shows that the grain boundaries in Wacker polysilicon are devoid of large barriers resulting from uncompensated charge.

Fig. 4.20 depicts the I-V characteristics of a representative device on Monsanto p-type polysilicon. Silver was used as an ohmic contact metal. The I-V characteristics show non-ohmic behaviour in high bias region. It can be seen that current across grain boundary decreases as the number of grain boundaries incorporated in between contacts increases. This can be due to the effect of grain boundary potential barriers on the carrier transport. Very high resistance in the linear region of

I-V characteristics has been observed. It can also be noted that the I-V characteristics are asymmetric and asymmetry exists even in case of two contacts without any grain boundary incorporated inbetween them. According to the simple model described in sec. 2.2.1 for carrier transport across grain boundary, this may not be due to grain boundary potential barrier. However, the transport properties of carriers can be considerably modified by the existance of additional barriers in the material arising due to various impurities and other defects, which are incorporated during the growth process. Also, it is probable that silver may be forming a low barrier on p-type polysilicon.

4.2.2 Effect of grain boundaries on electrical characteristics

Tables 4.5 and 4.6 contain representative experimental data obtained from MOS solar cells on n-type polysilicon with gold and silver as barrier metals. A number of cell arrays consisting of 0.5, and 1.0/mm dots have been fabricated to study the influence of grain boundaries on device parameters. The thickness of the barrier metal layer was varied between 50 and 120 Å. The contact was made to the dots with the help of a very sharp tip telescopic probe. The values of short-circuit current density, fill factor, and conversion efficiency of the cell could not be determined accurately because of the shadowing effect of the probe. The measured $\ln I_D$-V and $1/C^2$-V characteristics

of various dots in array Au 56 P, have been displayed in Fig. 4.21 and 4.22, respectively. Figures 4.23 and 4.24 depict the measured $\ln I_D$-V and $1/C^2$-V characteristics of various dots in array Ag 32 P. It is evident from Tables 4.5 and 4.6 that there is a weak influence of grain boundaries on open circuit voltage. However, in presence of large number of grain boundaries and defects, the value of open circuit voltage is considerably lower. The diode ideality factor seems to be higher in presence of grain boundaries. This may be due to higher value of recombination currents and a larger density of interface states [25]. The value of series resistance is not affected much by the grain structure. It can be observed that the value of barrier height obtained from $1/C^2$-V characteristics decreases with increasing number of grains, cf., Tables 4.5, and 4.6. This has also been reflected in the values of the barrier height obtained from the I_D-V data of array Ag 32 P, cf., Table 4.6. However, for array Au 56 P, the values of the barrier height obtained from the I_D-V data do not follow any particular trend, cf., Table 4.5. It can be noticed that the large values of barrier height and nice I_D-V characteristics are obtained on Wacker polysilicon. It may be expected that the grain boundaries will influence the collection efficiency of the photogenerated carriers. The influence of grain boundaries and other defects as recombination sites has been studied by a photon beam scanning arrangement. Large area MOS solar cells with diameter 5 to 7 mm have been fabricated on Wacker n-type polysilicon with gold and silver as barrier metals. The thickness of the barrier metal layer was varied between 50 and 120 Å. The photon-beam-induced current was measured as the sample was

scanned by a very fine beam of light of less than 0.5 mm in diameter. The variation of the light generated current observed has been about 7 to 9 percent in the region of large number of grain boundaries, while it was about 2 to 4 percent in the region of one or two grain boundaries. It can be noticed that the defect contribution to device performance by recombination mechanism is not pronounced for Wacker polysilicon material. This also has been observed earlier by C.V. Hari Rao et al [26].

Table 4.5: Influence of grain boundaries on various parameters of MOS polysilicon cells.

Device No. [Dot]	Dot located on	Dot Area (cm^2)	V_{oc} (mV)	Rs (Ohm. cm^2)	n	N_{doping} (cm^{-3})	Φ_F (V)	φ_1^o (V)	$\varphi_1^o+\Phi_F$ (V)	Φ_B (V)
Au 56F										
E3	1 grain	$2.0x10^{-3}$	373	0.47	1.50	$1.67x10^{15}$	0.25	0.64	0.89	0.77
B2	2 grains	$2.0x10^{-3}$	378	0.38	1.50	$1.67x10^{15}$	0.25	0.65	0.90	0.90
D1	2 grains + twin boundaries + defects	$2.0x10^{-3}$	376	0.52	1.66	$1.36x10^{15}$	0.26	0.62	0.88	0.78
D5	3 grains + twin boundaries	$1.3x10^{-3}$	362	0.46	1.66	$1.18x10^{15}$	0.26	0.60	0.86	0.76
B5	4 grains	$1.3x10^{-3}$	368	0.39	1.58	$1.67x10^{15}$	0.25	0.60	0.85	0.80

The polysilicon material was n-type (Wacker Chemitronic) and had a bulk resistivity of 1.0-10.0 Ohm. cm. Surface etching was carried out in a mixture of CF_4 and HNO_3 (1:1) for two minutes. Dry oxidation was carried out at 700°C for 60 seconds.

Table 4.6: Influence of grain boundaries on various parameters of MOS polysilicon cells.

Device No. [Dot]	Dot located on	V_{oc} (mV)	Rs (Ohm.-cm^2)	n	N_{doping} (cm^{-3})	Φ_F (V)	φ^o_i (V)	$\varphi^o_i + \Phi_F$ (V)	Φ_B (V)
Ag 32P									
.33	1 grain	387	0.21	1.33	1.92×10^{15}	0.25	0.67	0.92	0.88
A3	3 grains	384	0.18	1.42	1.94×10^{15}	0.25	0.62	0.87	0.85
B1	4 grains	390	0.18	1.50	1.83×10^{15}	0.25	0.64	0.89	0.85
C2	5 grains + twin boundaries	370	0.21	1.58	1.96×10^{15}	0.25	0.60	0.85	0.82

The polysilicon material was n-type (Wacker Chemitronic) and had a bulk resistivity of 1.0 - 10.0 Ohm. cm. Surface etching was carried out in a mixture of CP4 and HNO_3 (1:1) for two minutes. Dry oxidation was carried out at 700 °C for 60 seconds. The dot area was 7.9×10^{-3} cm^2.

5. CONCLUSIONS

MOS diodes were fabricated both on single crystal and polysilicon substrates with an interfacial layer thickness of about 20 Å. The barrier metal was Au on n-type silicon, and Al on p-type silicon. The carrier transport mechanisms in these devices were investigated by carrying out measurements of diode current-voltage characteristics and capacitance-voltage characteristics at various temperatures. The activation energy analysis was carried out by plotting $\ln J_o$ as a function of $1/T$, and $1/nT$. Plots of $\ln J_o$ vs T were also made. In all these devices, the values of silicon band bending at zero bias, obtained from $1/C^2$-V characteristics showed a decrease with increasing temperature. In Al MOS diodes on p-type single crystal silicon, the change in φ_i^o with temperature was more or less explained by decrease in the bandgap, and shift in the Fermi level position. However, in MOS diodes on polysilicon substrate, it was observed that the total change in φ_i^o over the temperature range of study, was larger than that observed in case of Al MOS diodes on single crystal silicon. This change in φ_i^o could not be accounted for by the decrease in the silicon bandgap and the change in bulk Fermi level with temperature. From, experimental data, $(\varphi_i^o + \phi_F)$ was also found to decrease with increasing temperature. This behaviour of $(\varphi_i^o + \phi_F)$ could not be explained by considering the change in interface state charge with the change in Fermi level position with temperature.

In case of Al MOS diodes on p-type single crystal silicon, $\ln J_o$ vs 1/T and 1/nT plots were found to be equally linear. The variation of $\ln J_o$ with temperature was a non linear function. This indicated the absence of field emission component. Also, the nature of nkT/q vs kT/q plot revealed that thermionic emission may be the dominant transport mechanism. However, the value of the barrier height obtained from the saturation current value, assuming thermionic emission, was found to increase with temperature. This was quite opposite to the behaviour of $(\varphi_1^p + \phi_F)$ with temperature. The results indicated the difficulty encountered in analysizing results. One common feature observed in devices on polysilicon was that, the $\ln J_o$ vs T plot was always linear. This indicated the presence of a tunneling component in MOS diodes fabricated on polysilicon. In case of Al MOS diodes on p-type polysilicon, and in one set of Au MOS diodes on n-type polysilicon, $\ln J_o$ was found to be linear with respect to 1/nT rather than 1/T. This together with the nature of $\ln J_o$ vs 1/T and $\ln J_o$ vs 1/nT plots showed that thermionic field emission could be the dominant transport mechanism. The nature of nkT/q vs kT/q plots might lead one to believe that, thermionic emission could be the dominant mechanism. However, it should be noted that in presence of thermionic field emission, the plot of nkT/q vs kT/q deviates from linearity in low temperature range. But, at higher temperatures, the nature of this plot does not differ from that for thermionic emission. An unusual feature was observed in the $\ln I_D$-V

characteristics of some Au MOS diodes on polysilicon. The following typical behaviour was noticed for these devices. The decrease in φ_1^o was very large, and nT was constant rather than n. Also , the plot of $\ln J_o$ vs 1/T was strongly non linear. The variation of $\ln J_o$ with T was linear. From the nature of these plots and experimental data, it was concluded that thermionic emission, thermionic field emission, or minority carrier injection could not be the dominant transport mechanism. In these devices, the change in I_D with temperature could be explained by the corresponding variation of φ_1^o. The observed behaviour in these devices was similar to what had been noticed by several workers earlier [5,19-21], and indicated the possibility of multistep tunneling through the silicon space charge layer as the dominant transport mechanism in presence of large number of traps in polysilicon material. From the experimental data collected , and on the basis of theoretical discussion, it became clear that the dominant transport mechanism could depart from thermionic emission to thermionic field emission to multistep tunneling depending upon the magnitude of φ_i^o and presence of traps in the silicon space charge layer. The study also stressed that sufficient caution should be exercized before drawing any firm conclusion about the dominant carrier transport mechanism. The study of grain boundary potential barriers revealed that, Wacker polysilicon material is devoid of large potential barriers. The measured I-V characteristics showed an ohmic behaviour, and the resistance involved was accounted for by the bulk resistivity of the material. Similar studies on Monsanto polysilicon material indicated the

possible existance of grain boundary potential barriers. From the studies carried out to investigate the influence of grain boundaries on electrical parameters of solar cell, it was found that the grain boundaries had only a weak influence on open circuit voltage, diode ideality factor, series resistance, and barrier height in silicon. Similar results had been reported earlier by S. Bhattacharya et al [25]. The influence ofgrain boundaries on photogenerated carriers was investigated by a photon beam scanning arrangement, and it was observed that the variation of light generated current was not significant in grainboundary regions. These types of studies established that, MOS structures with their inherent advantages over p-n junction configuration, could be used profitably on Wacker polysilicon material for photovoltaic applications.

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FIGURE CAPTIONS

Fig. 2.1 Energy band diagram of an MOS diode on p-type silicon.

Fig. 2.2 Energy band diagram describing two semi-infinite silicon grains and one grain boundary
(a) before joining,
(b) after joining.

Fig. 3.1 Sequence of the fabrication steps for various devices.

Fig. 3.2 Circuit diagram of the set-up used for measuring
(a) diode current-voltage characteristics,
(b) capacitance-voltage characteristics.

Fig. 3.3 Arrangement for photon beam scanning.

Fig. 4.1 Measured diode current-voltage characteristics of MOS diode Al 1 B2 at different temperatures.

Fig. 4.2 Experimental plots of ln J_0 vs 1/T and 1/nT for MOS diode Al 1 B2.

Fig. 4.3 Experimental plot of lnJ_0 vs T for MOS diode Al 1 B2.

Fig. 4.4 Measured $1/C^2$ vs V characteristics of MOS diode Al 1 B2 at different temperatures.

Fig. 4.5 Measured diode current-voltage characteristics of MOS diode Al 25P C3 at different temperatures.

Fig. 4.6 Experimental plots of lnJ_0 vs 1/T and 1/nT for MOS diode Al 25P C3.

Fig. 4.7 Experimental plot of lnJ_0 vs T for MOS diode Al 25P C3.

Fig. 4.8 Measured $1/C^2$ vs V characteristics of MOS diode Al 25P C3 at different temperatures.

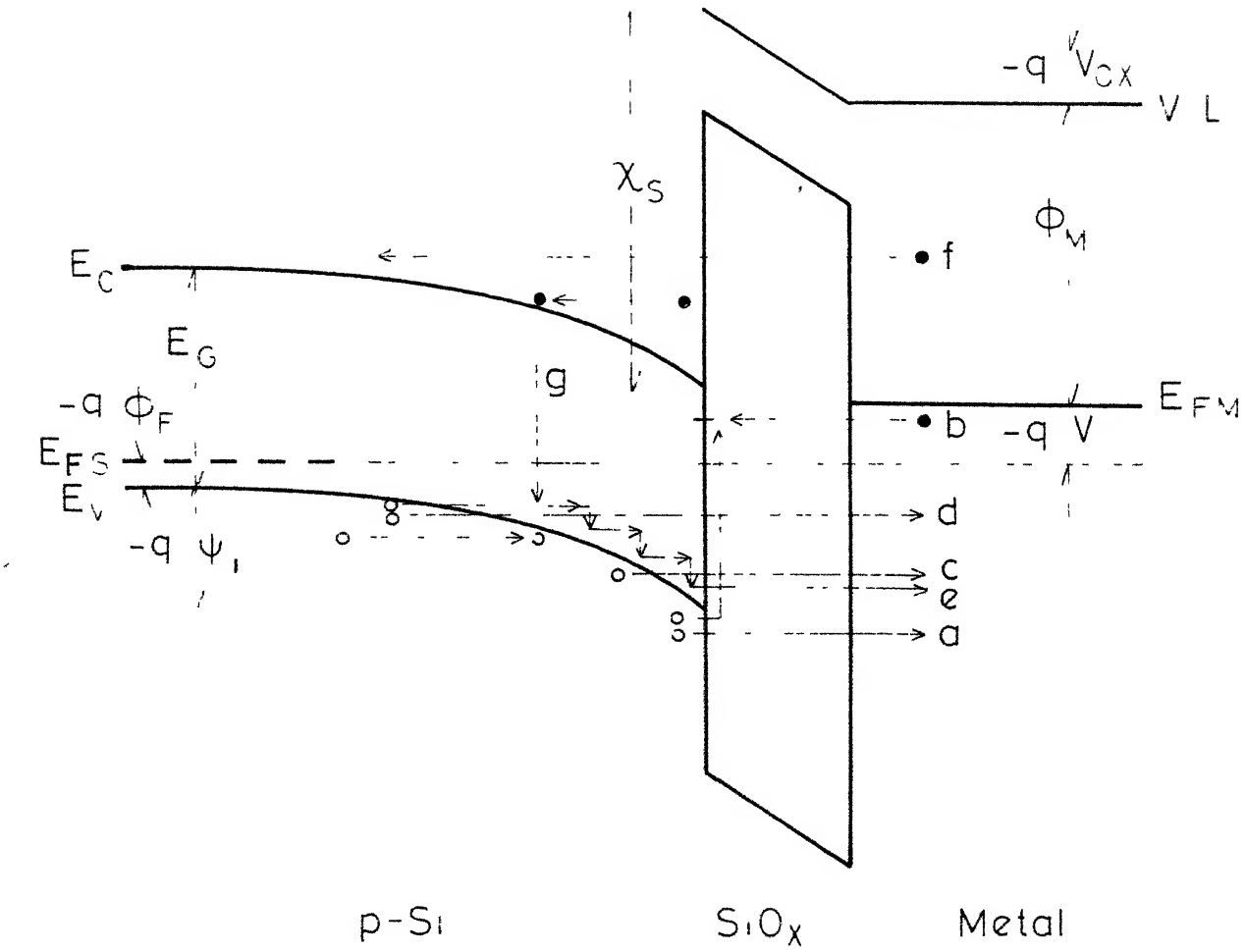


Fig 2 1

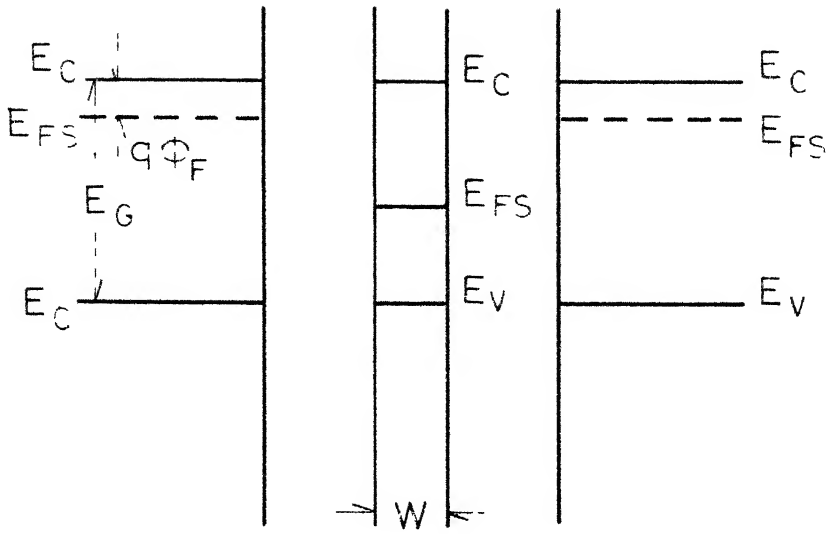


Fig 22a

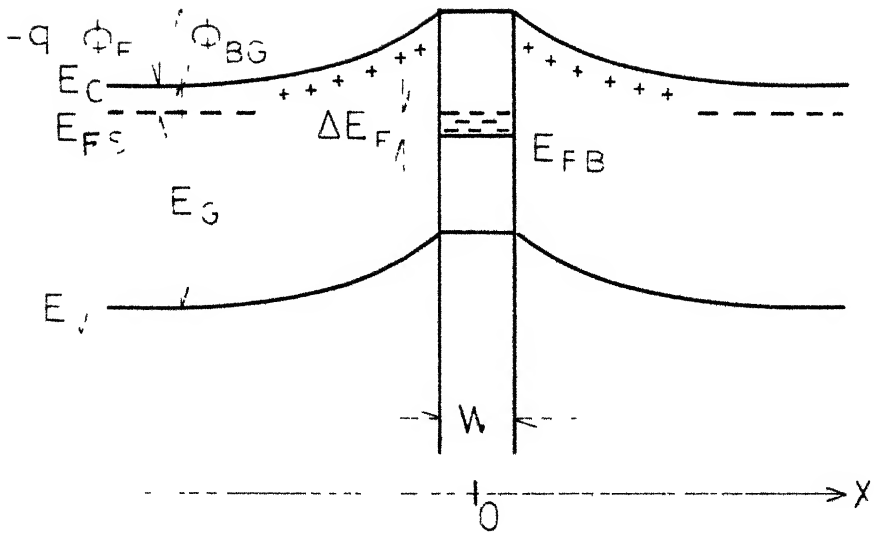


Fig 22b

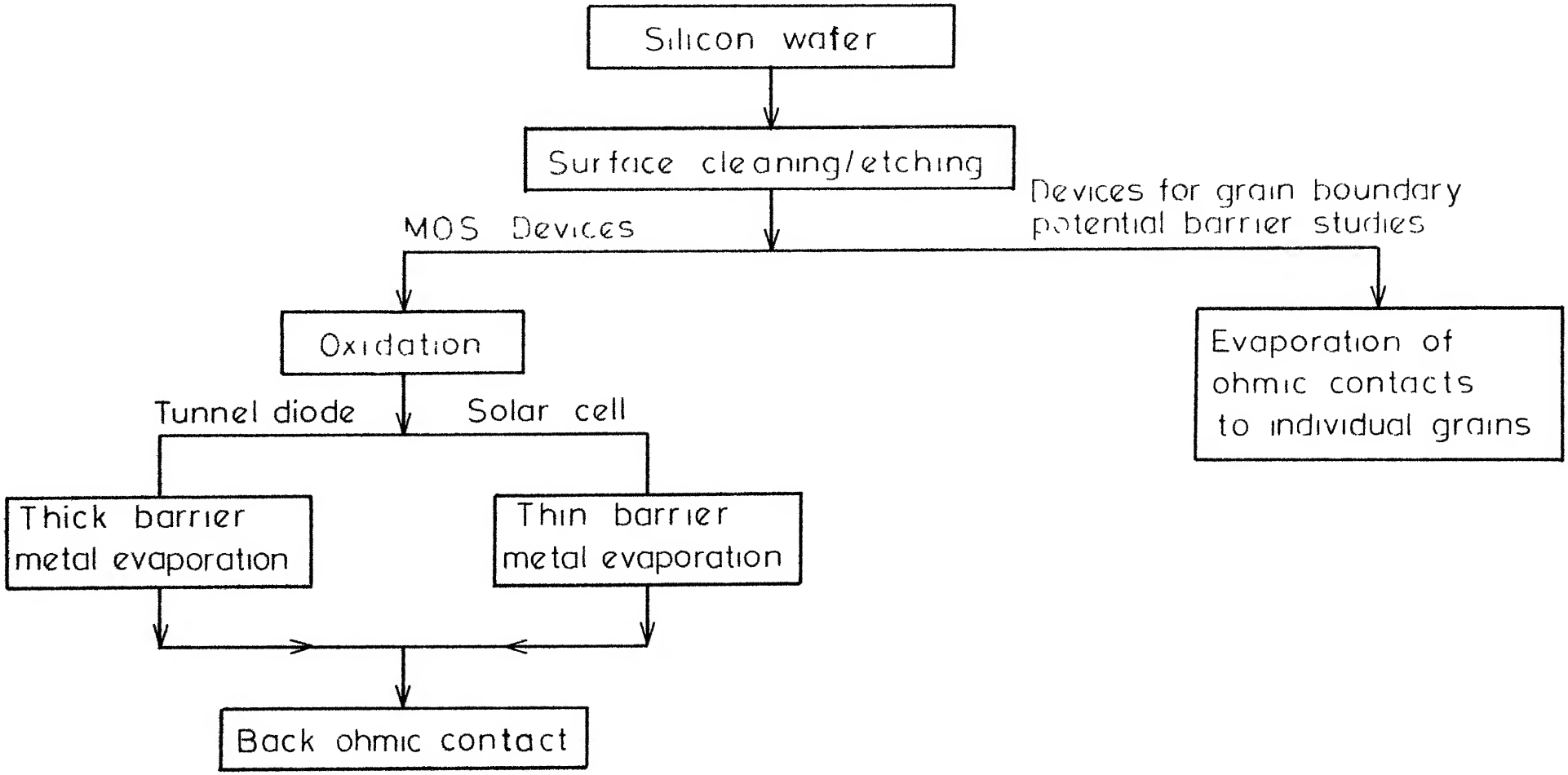

Silicon wafer
Surface cleaning/etching
MOS Devices
Devices for grain boundary potential barrier studies
Oxidation
Evaporation of ohmic contacts to individual grains
Tunnel diode
Solar cell
Thick barrier metal evaporation
Thin barrier metal evaporation
Back ohmic contact

Fig 3 1

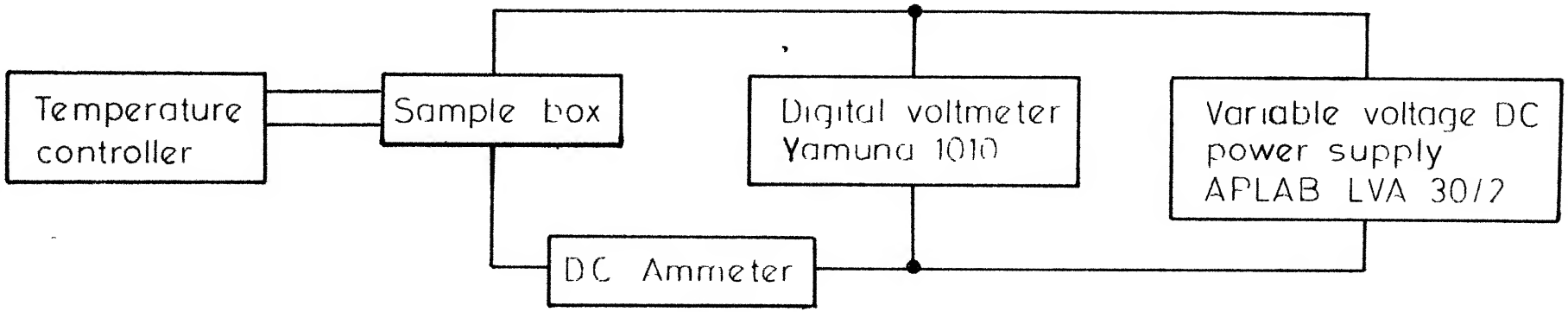


Fig 3 2 a

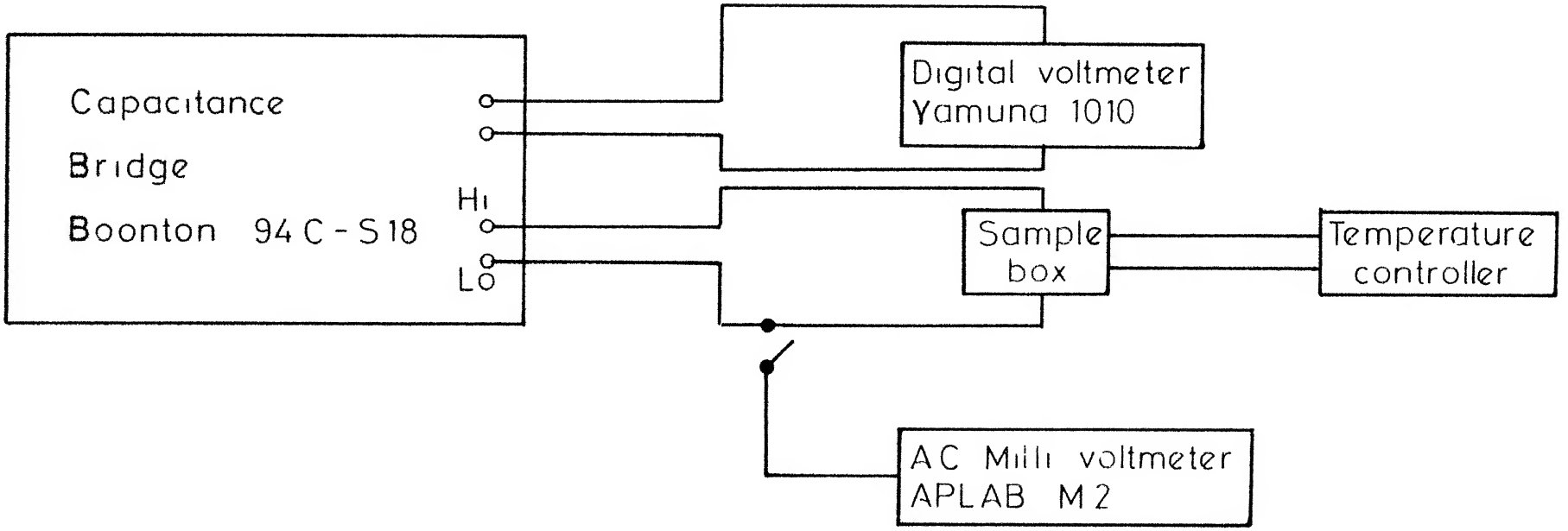


Fig 3 2 b

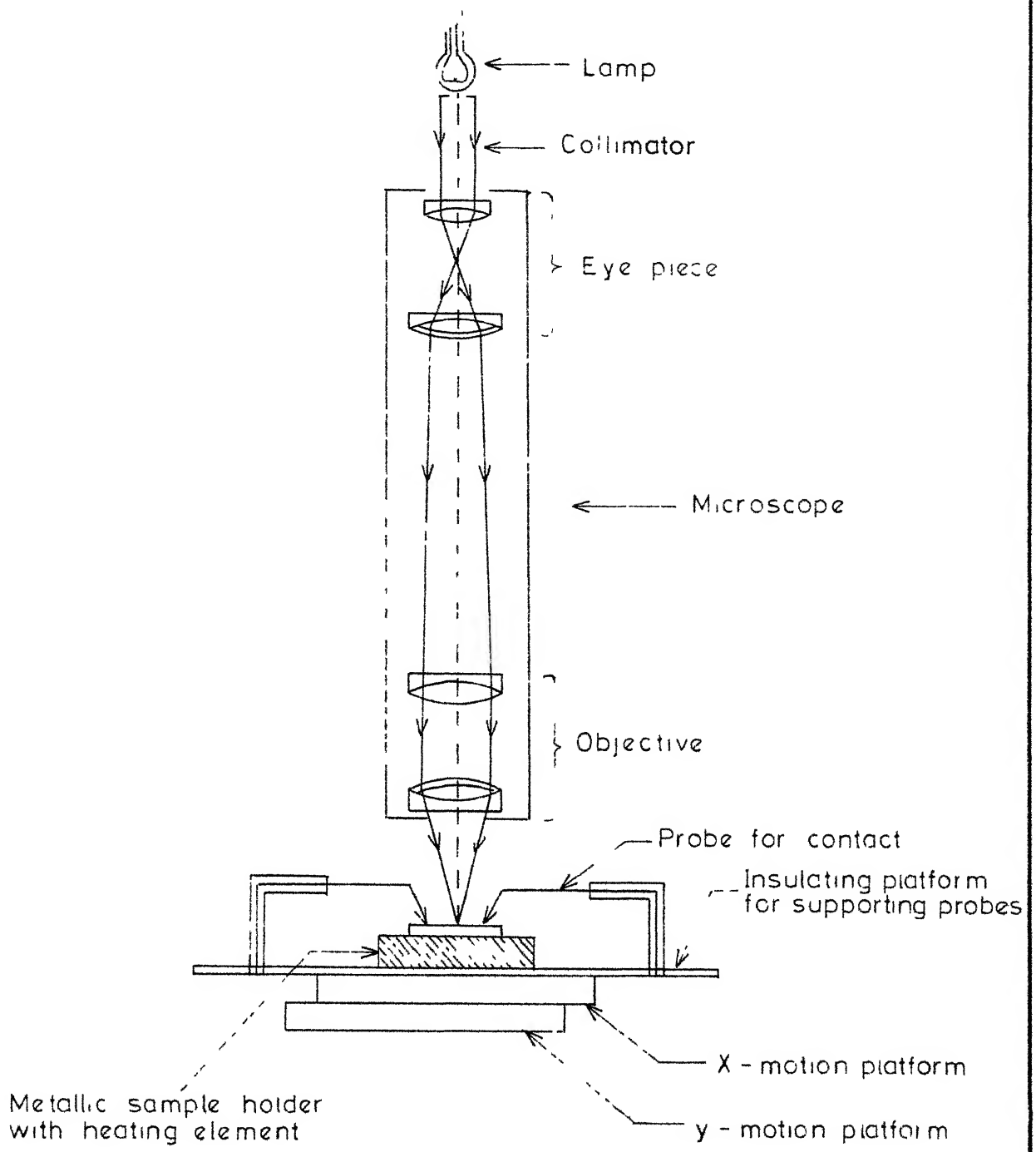
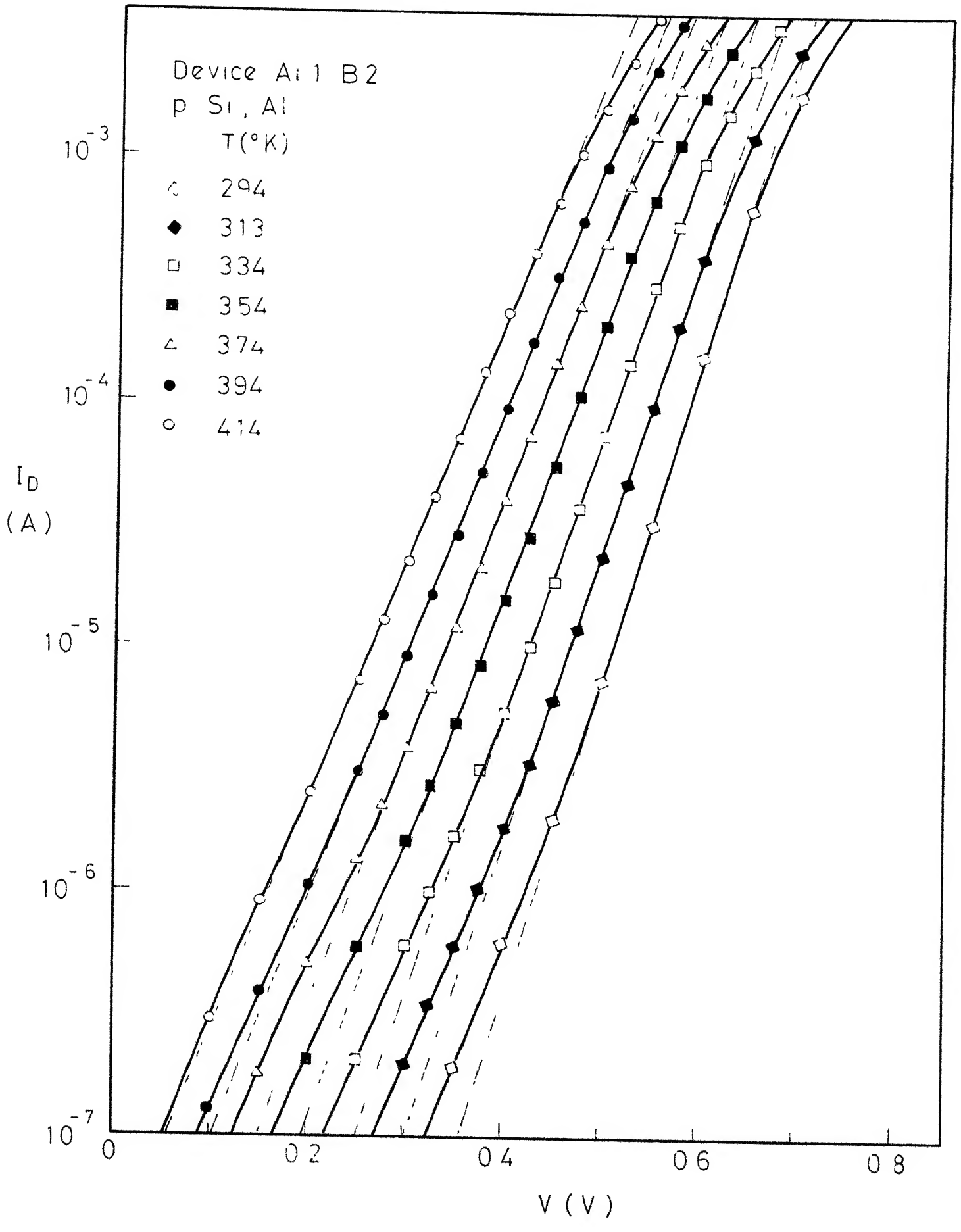

Lamp
Collimator
Eye piece
Microscope
Objective
Probe for contact
Insulating platform
for supporting probes
X - motion platform
y - motion platform
Metallic sample holder
with heating element

Fig 3 3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313
334
354
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394
414
10^{-3}
10^{-4}
10^{-5}
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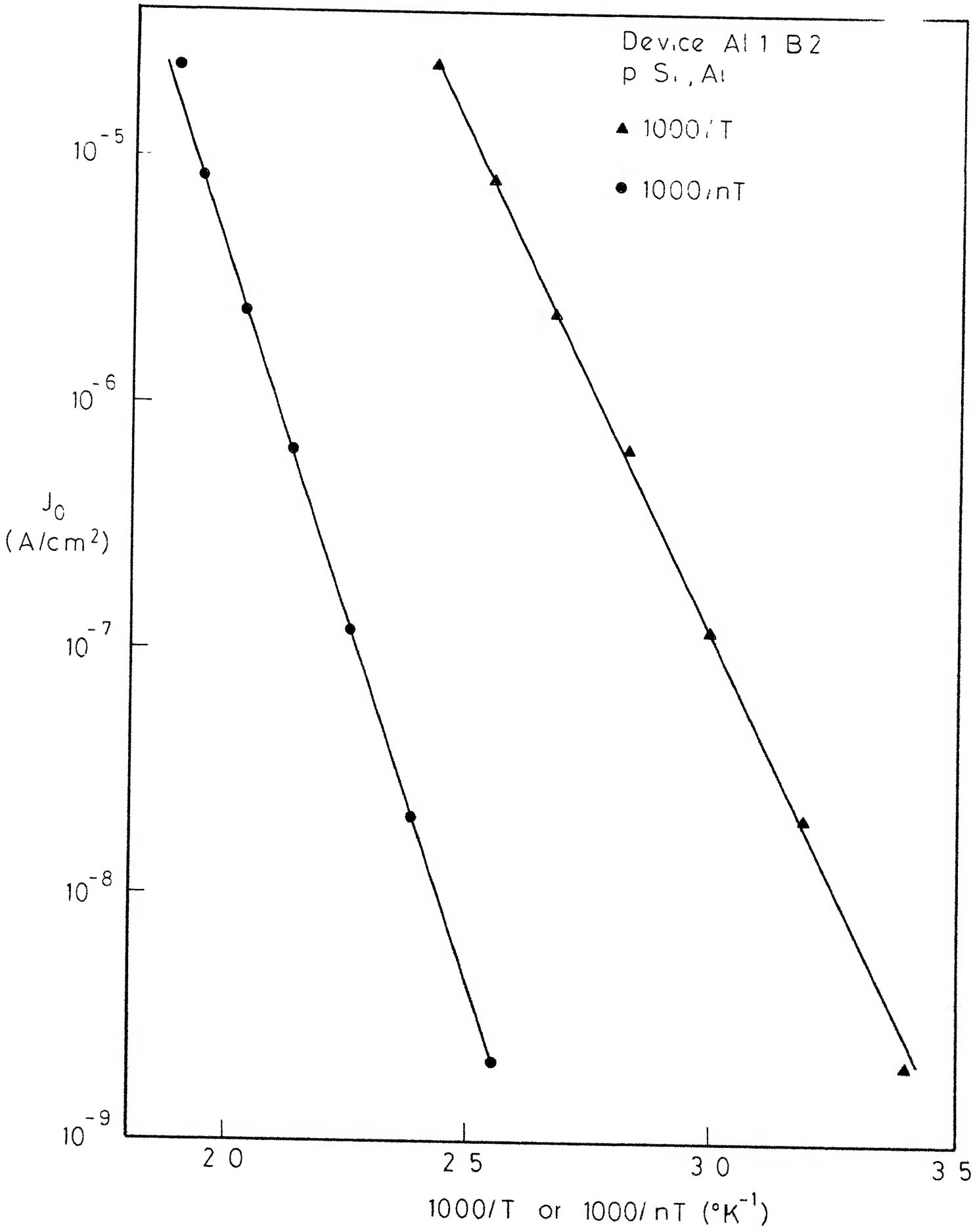
10^{-7}
I_D
(A)
0
0 2
0 4
0 6
0 8
V (V)

Fig 4 1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● 1000/nT
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10^{-6}
10^{-7}
10^{-8}
10^{-9}
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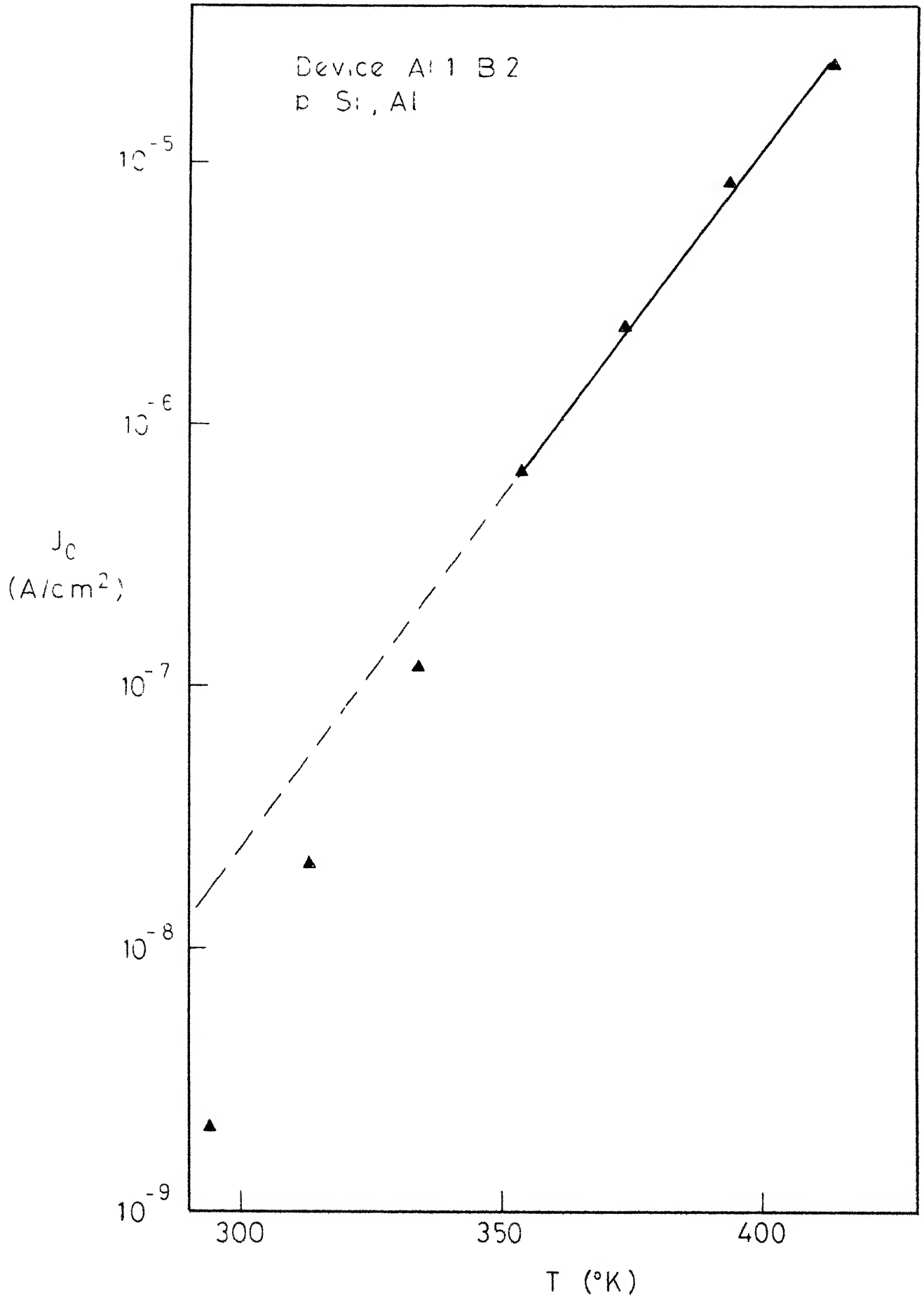
30
35
1000/T or 1000/nT (°K⁻¹)

Fig 4.2



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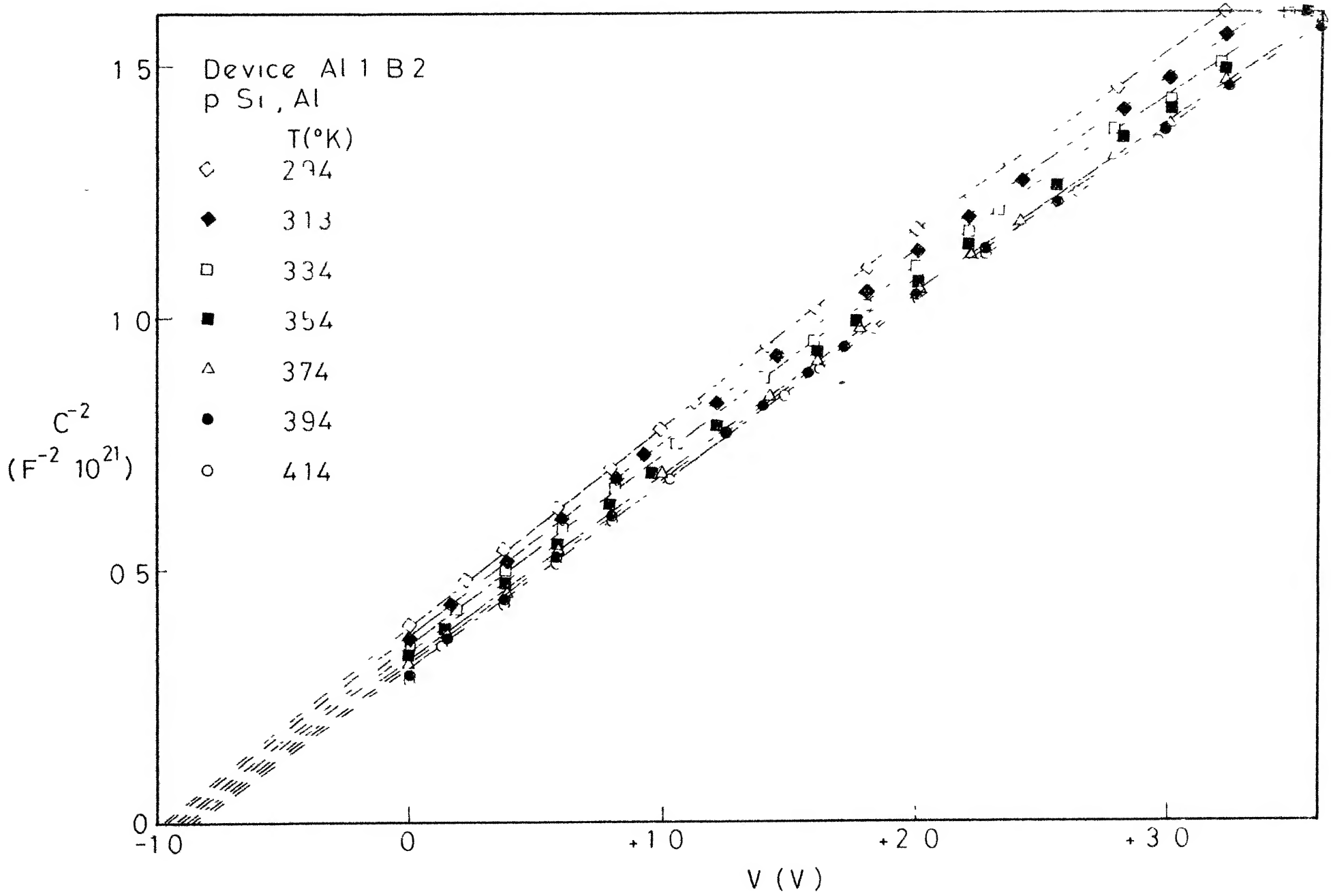
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T(°K)
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313
334
354
374
394
414
1 5
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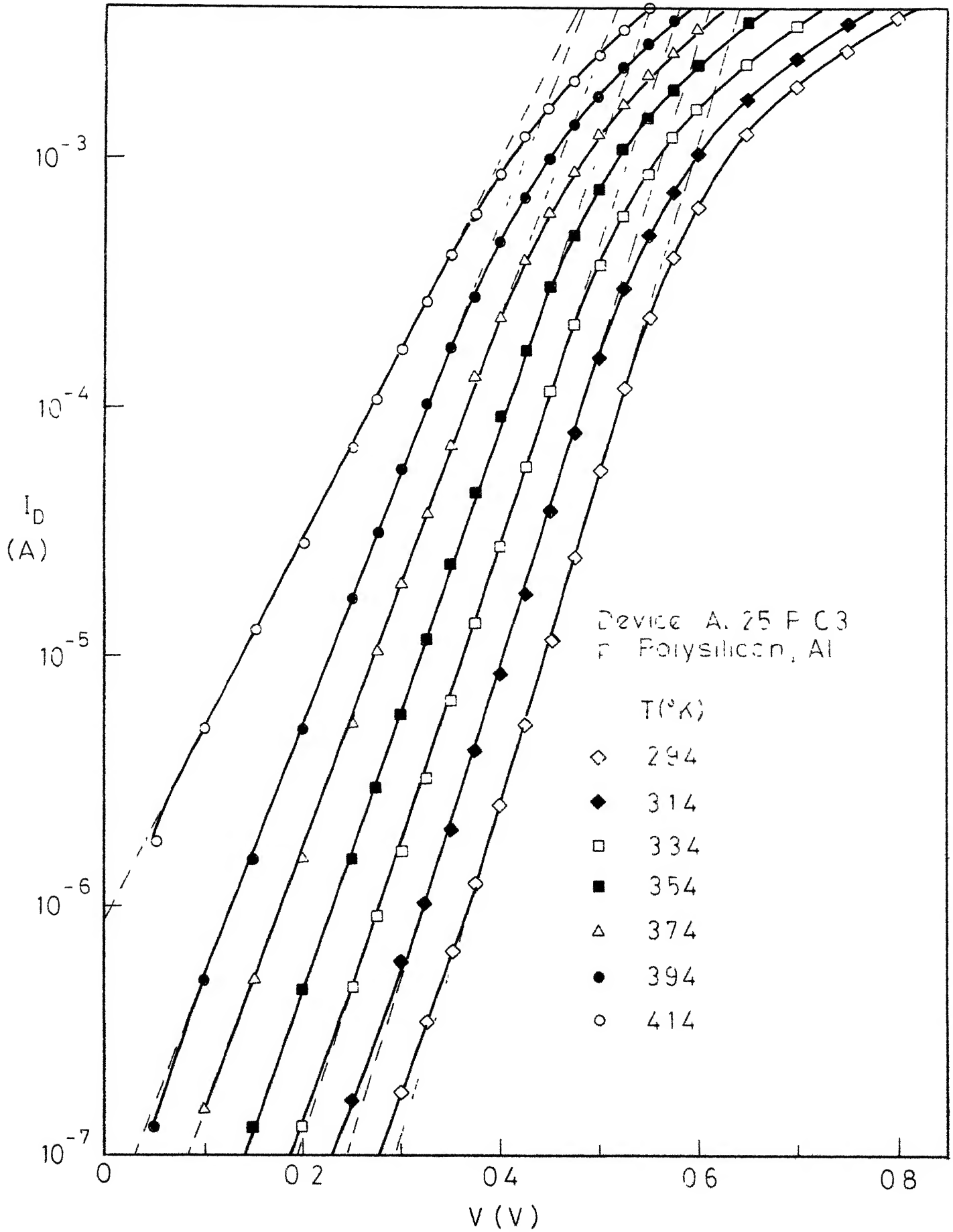
0 5
0
C^{-2}
$(F^{-2}\ 10^{21})$
-10
0
+10
+20
+30
V (V)

Fig 4 4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(A)
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0 2
0 4
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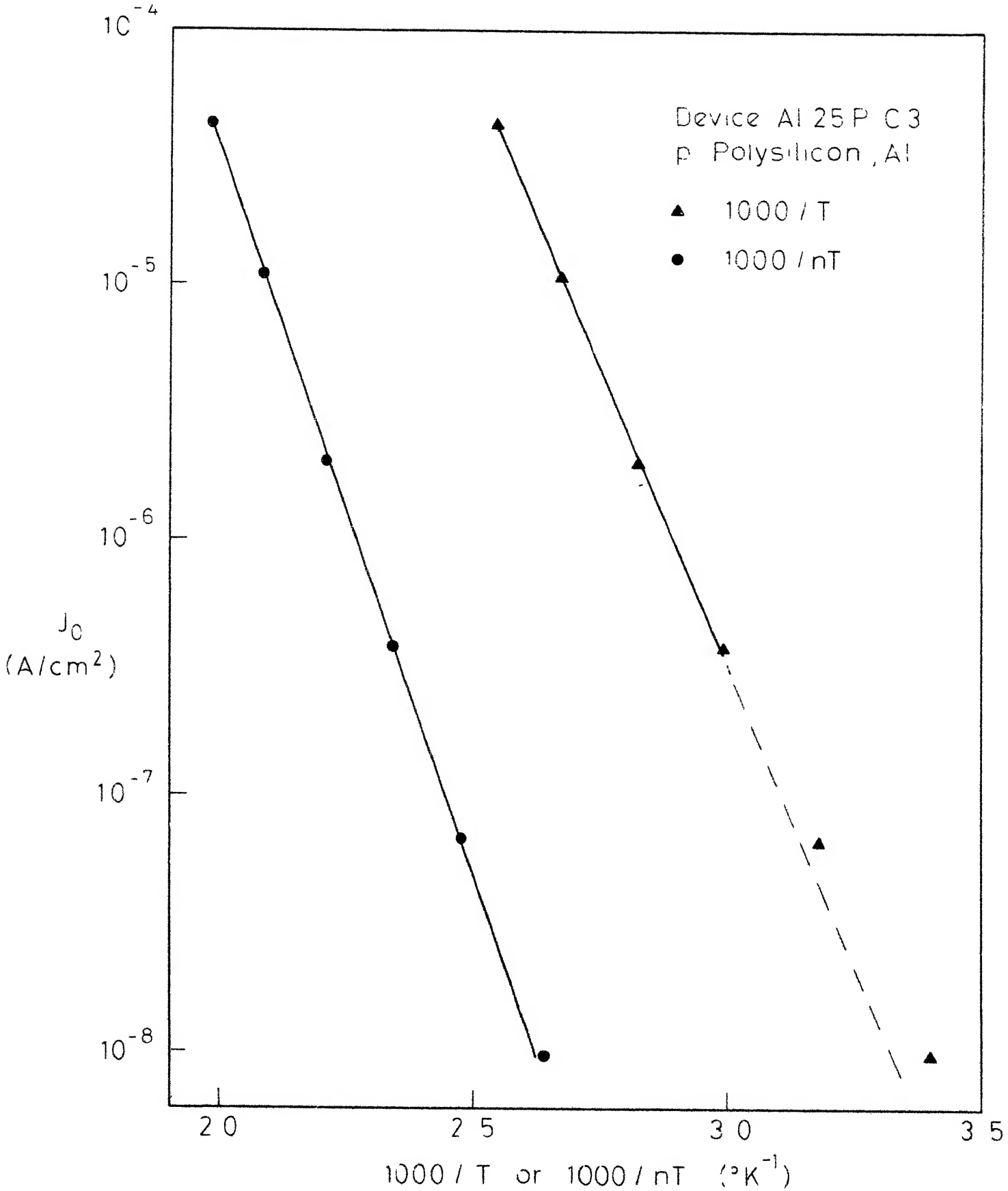
0 8
V (V)
Device A. 25 F C3
F Polysilicon, Al
T(°K)
294
314
334
354
374
394
414

Fig 4 5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10^{-5}
10^{-6}
10^{-7}
10^{-8}
J_0
(A/cm²)
20
25
30
35
1000 / T or 1000 / nT (°K⁻¹)

Fig 4 6

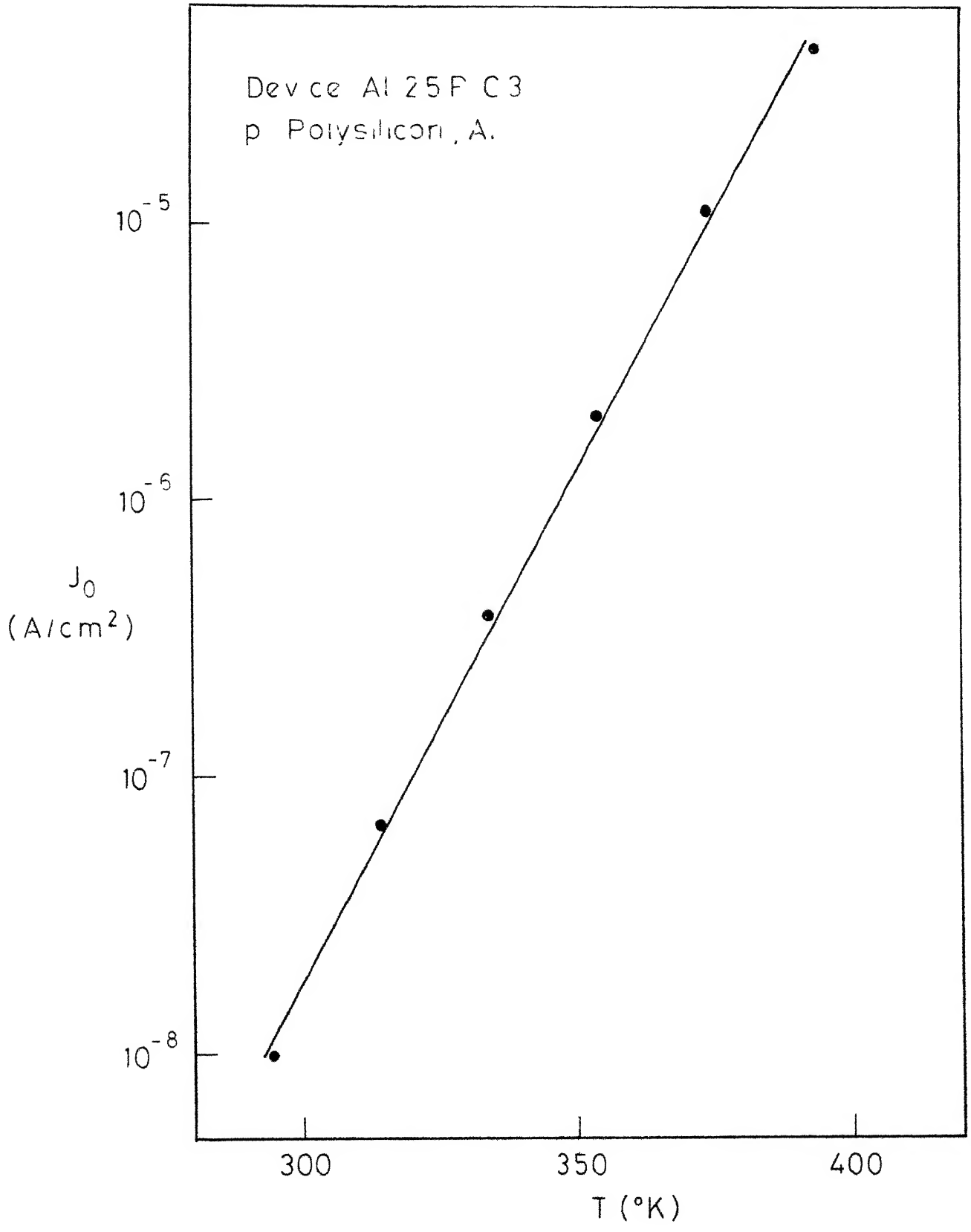
Device A1 25F C3
p Polysilicon, A.
10^{-5}
10^{-6}
10^{-7}
10^{-8}
J_0
(A/cm^2)
300
350
400
T (°K)

Fig 4 7

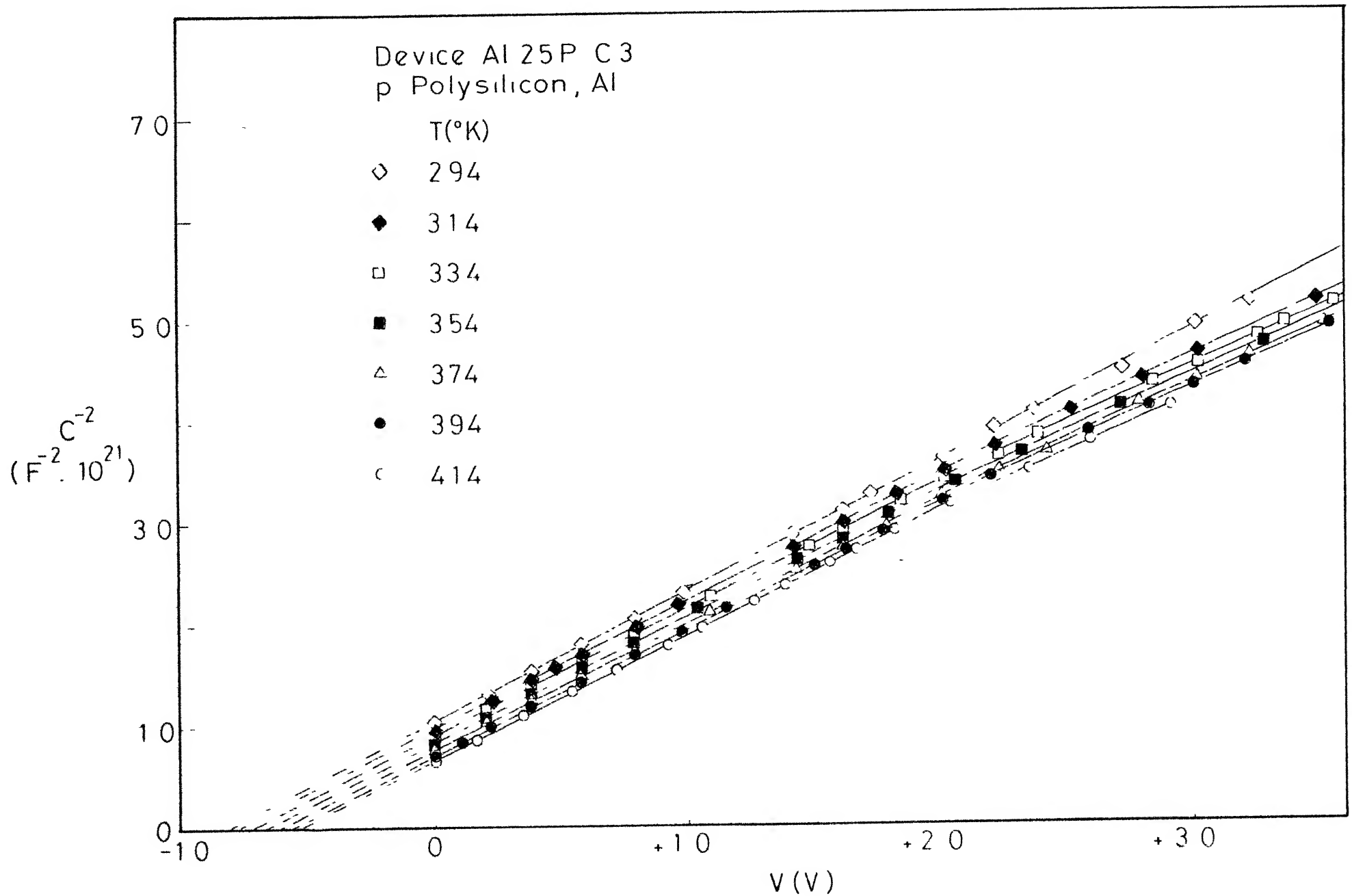
Device Al 25P C3
p Polysilicon, Al
T(°K)
294
314
334
354
374
394
414
C^-2
(F^-2 . 10^21)
70
50
30
10
0
-10
0
+10
+20
+30
V(V)

Fig 4 8

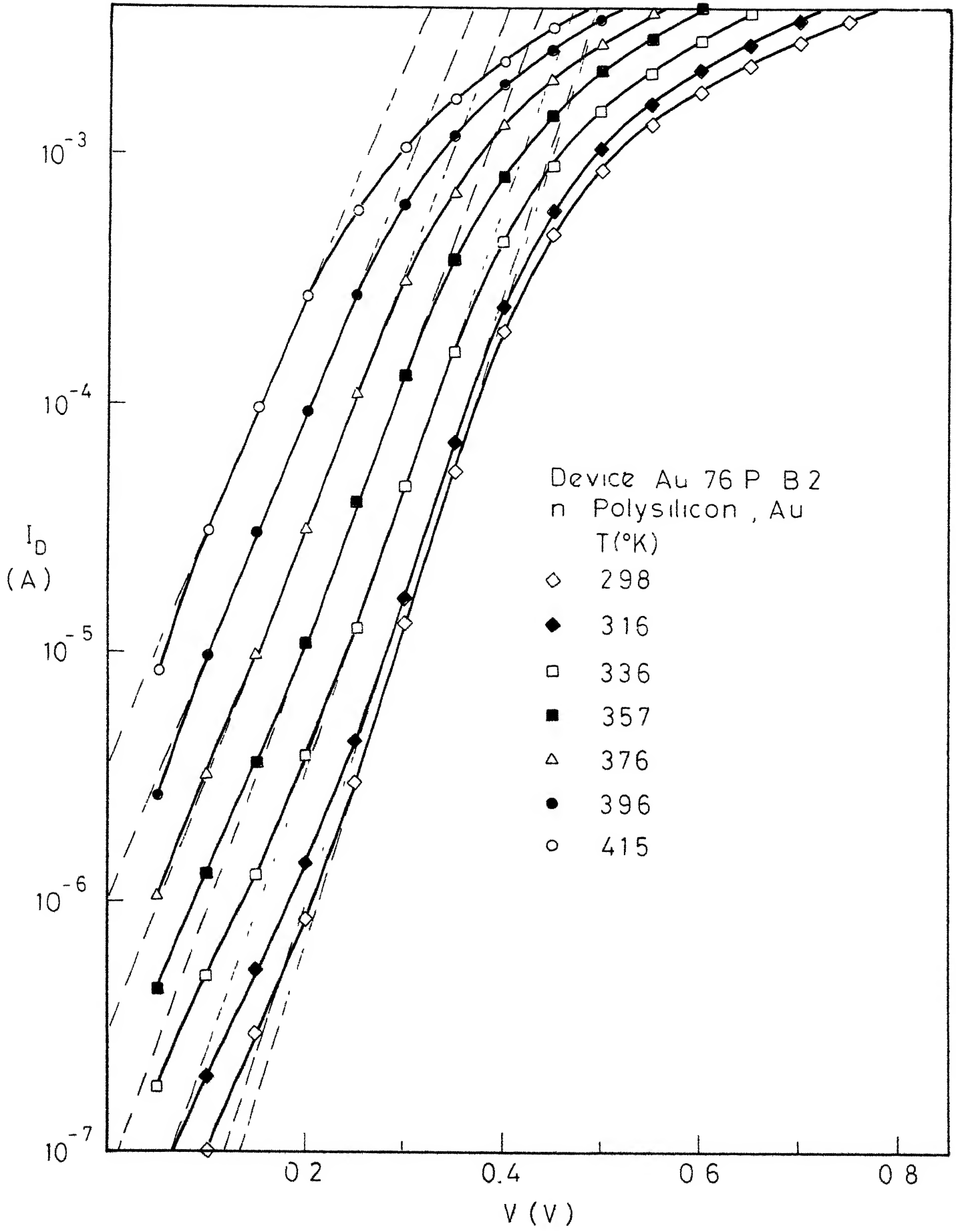
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
I_D
(A)
0 2
0.4
0 6
0 8
V (V)
Device Au 76 P B 2
n Polysilicon , Au
T(°K)
298
316
336
357
376
396
415

Fig 4 9

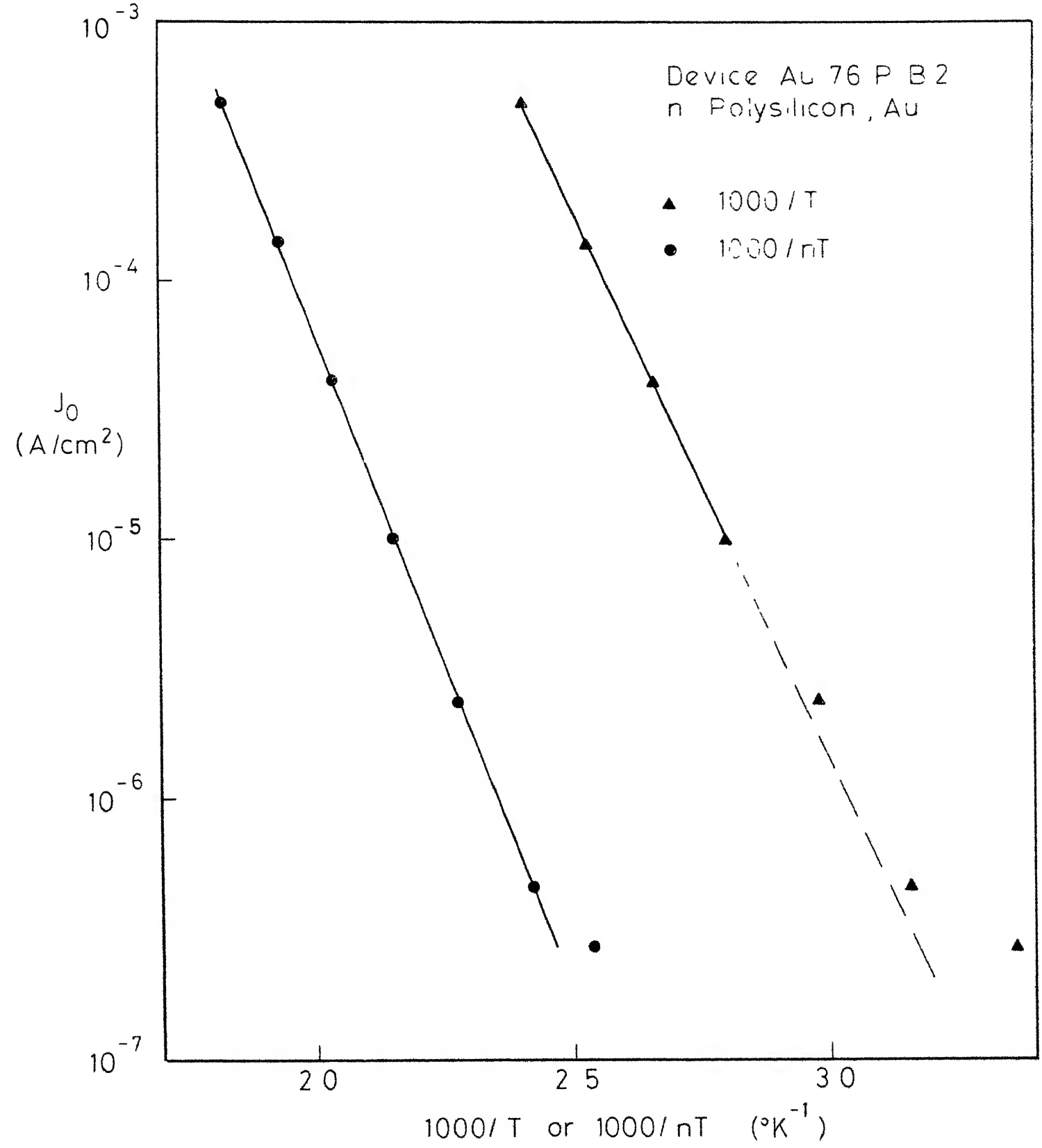
Device Au 76 P B 2
n Polysilicon , Au
1000 / T
1000 / nT
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
J_0
(A/cm^2)
20
25
30
1000/ T or 1000/ nT (°K^{-1})

Fig 4 10

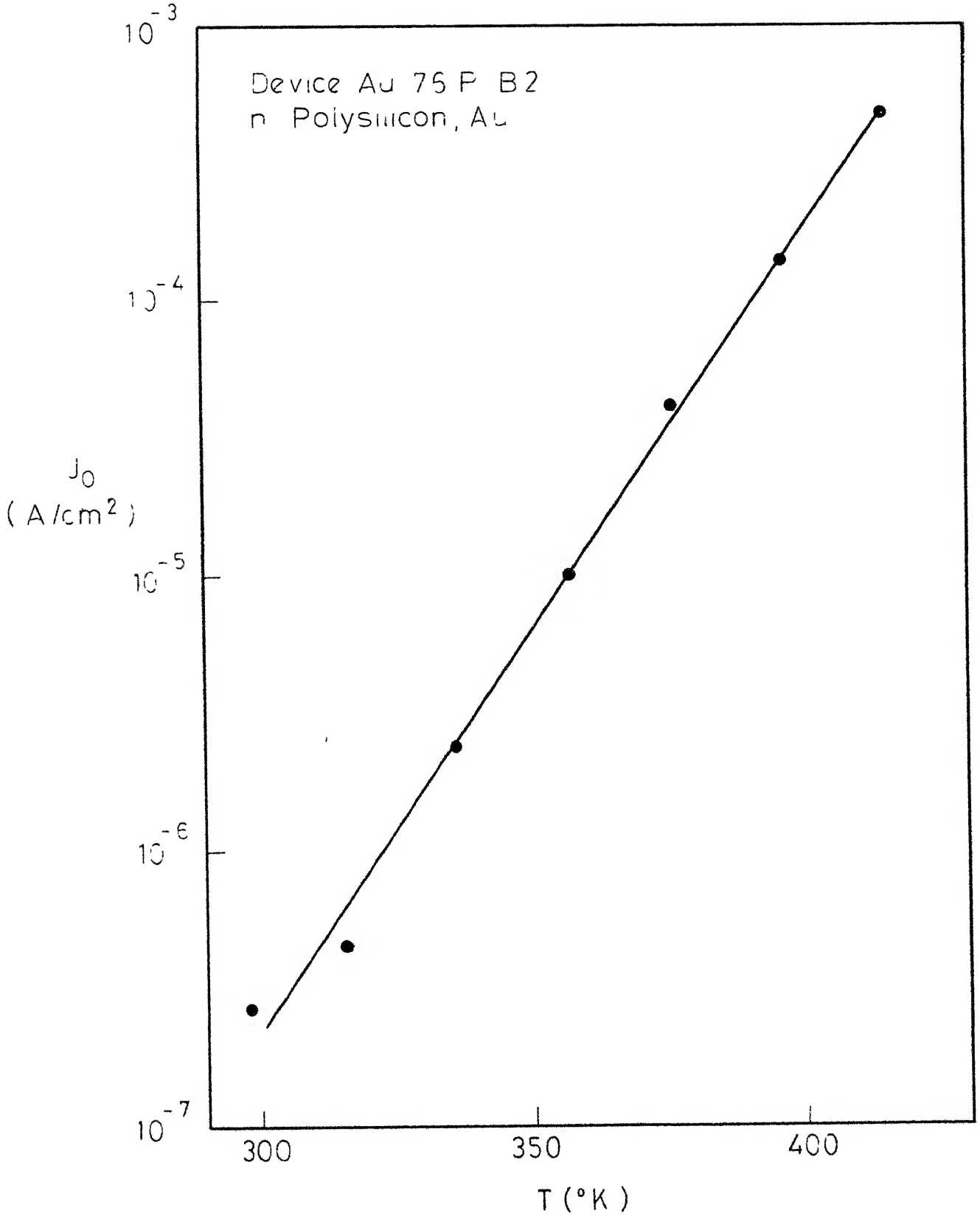
Device Au 75 P B2
n Polysilicon, Au
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
J_0
(A/cm^2)
300
350
400
T (°K)

Fig 4 11

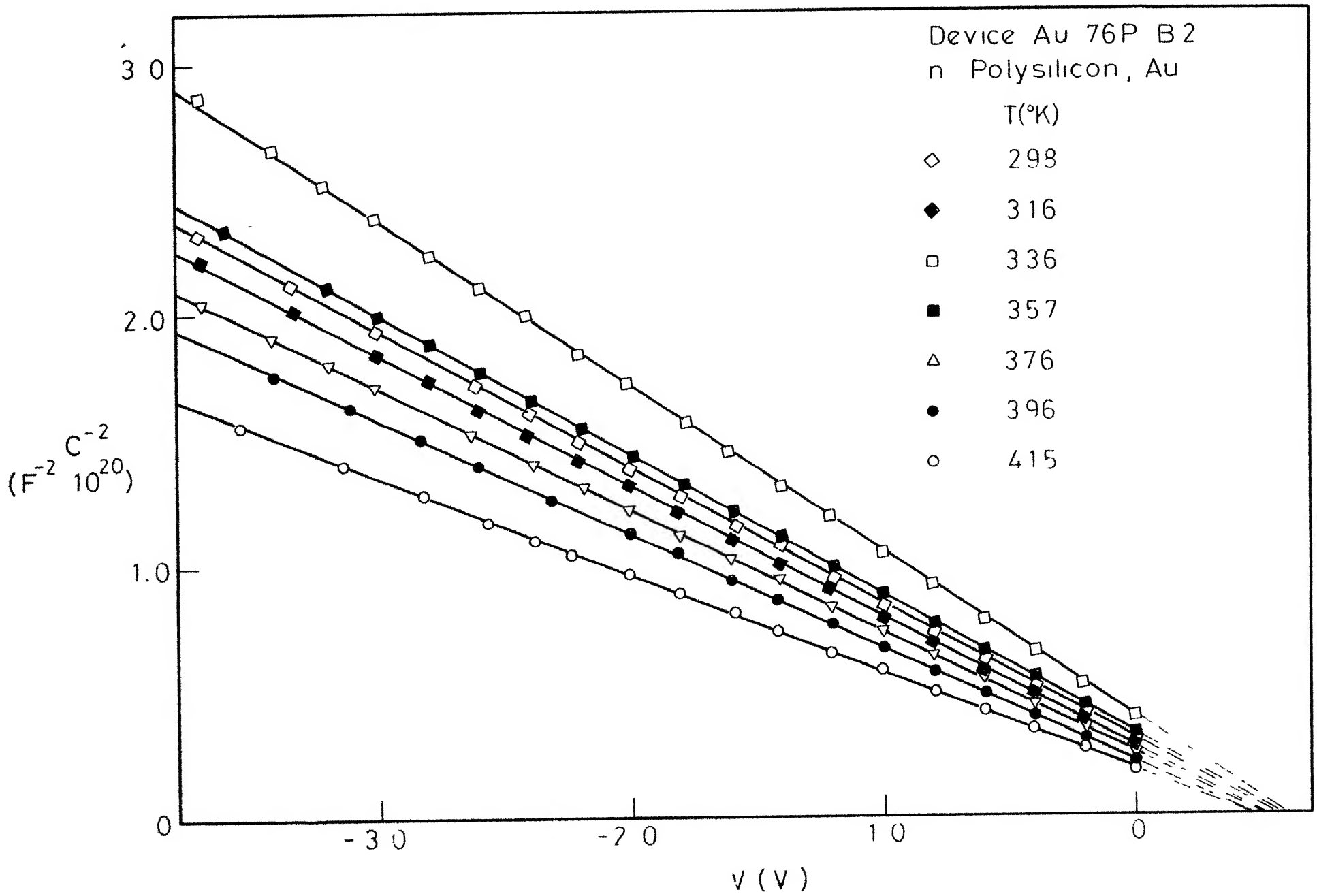
Device Au 76P B2
n Polysilicon, Au
T(°K)
298
316
336
357
376
396
415
3 0
2.0
1.0
0
C^-2
(F^-2 10^20)
-3 0
-2 0
1 0
0
V (V)

Fig 4 12

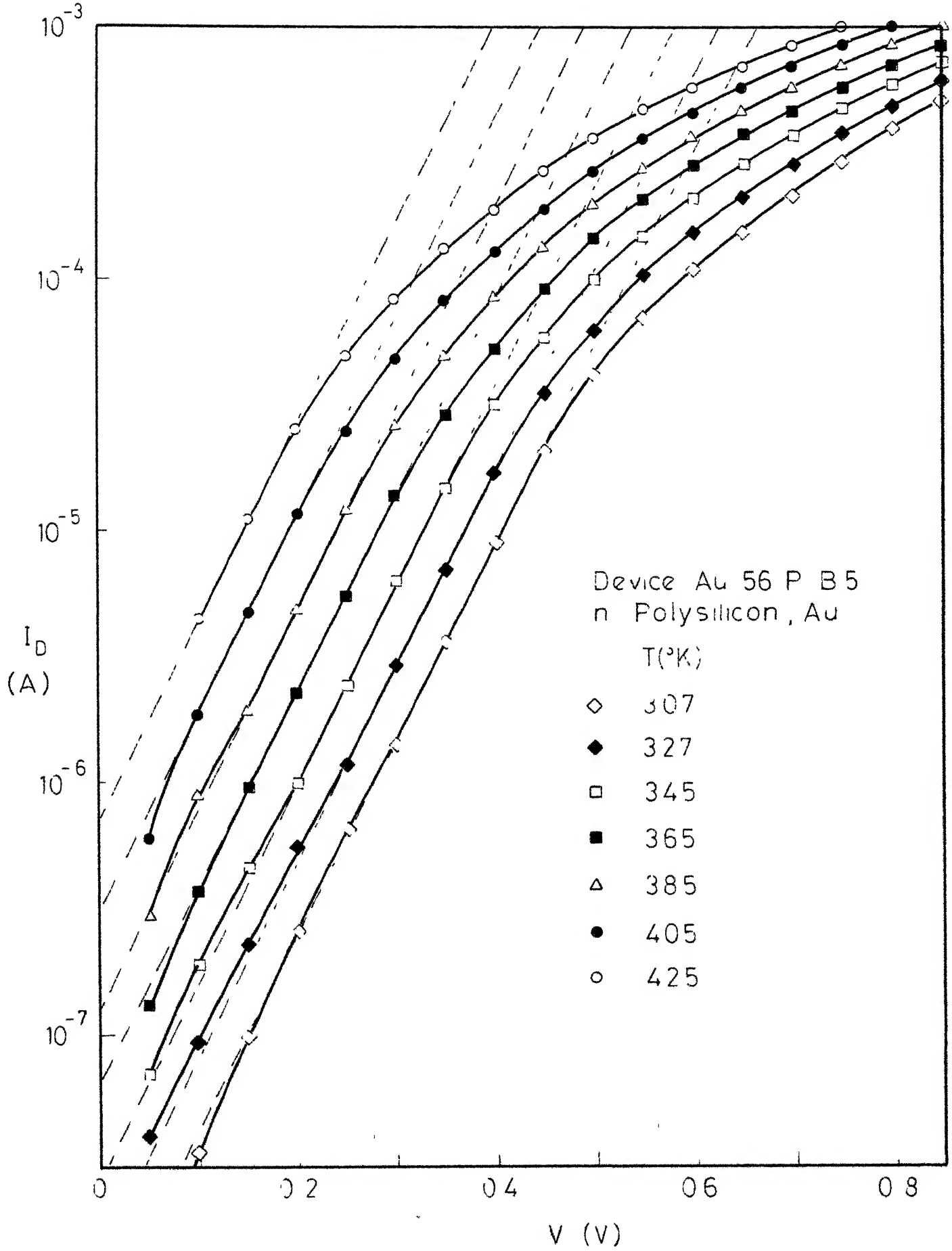
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
I_D
(A)
Device Au 56 P B 5
n Polysilicon, Au
T(°K)
307
327
345
365
385
405
425
0
0 2
0 4
0 6
0 8
V (V)

Fig. 4 13

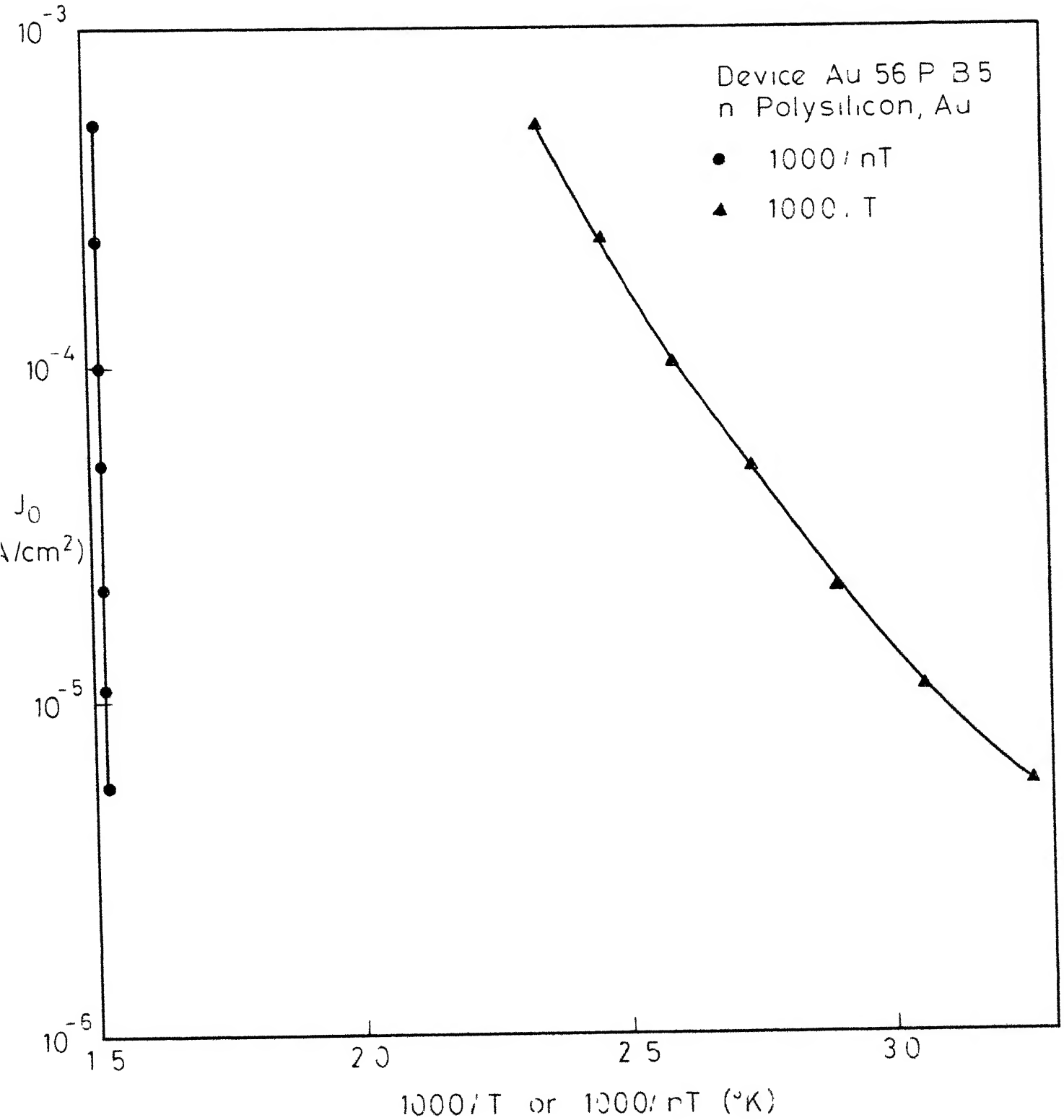
Device Au 56 P B5
n Polysilicon, Au
1000/nT
1000/T
10^{-3}
10^{-4}
10^{-5}
10^{-6}
J_0
A/cm^2)
1 5
2 0
2 5
3 0
1000/T or 1000/nT (°K)

Fig 4 14

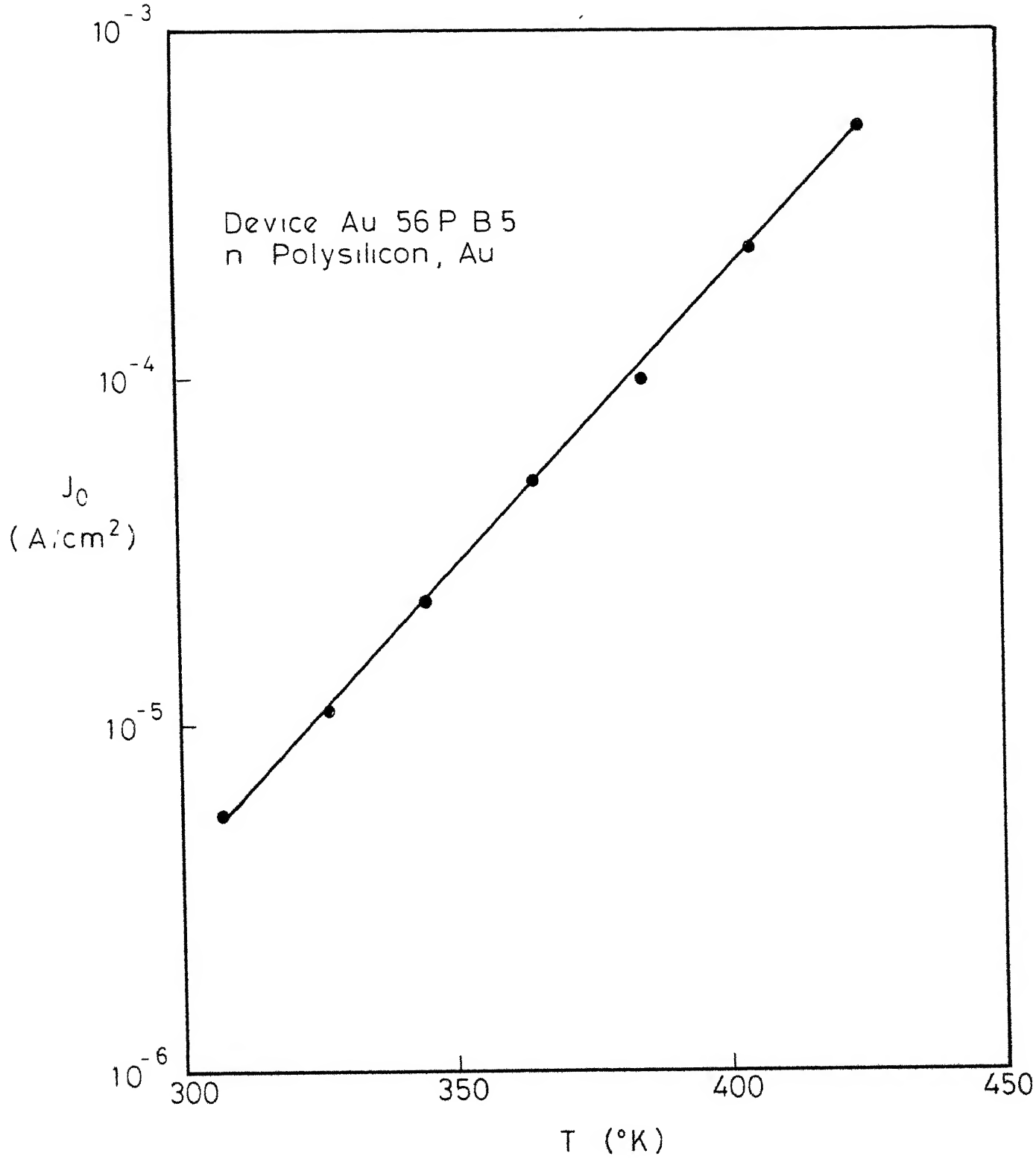
Device Au 56 P B 5
n Polysilicon, Au
10^{-3}
10^{-4}
10^{-5}
10^{-6}
J_0
(A/cm^2)
300
350
400
450
T (°K)

Fig 4.15

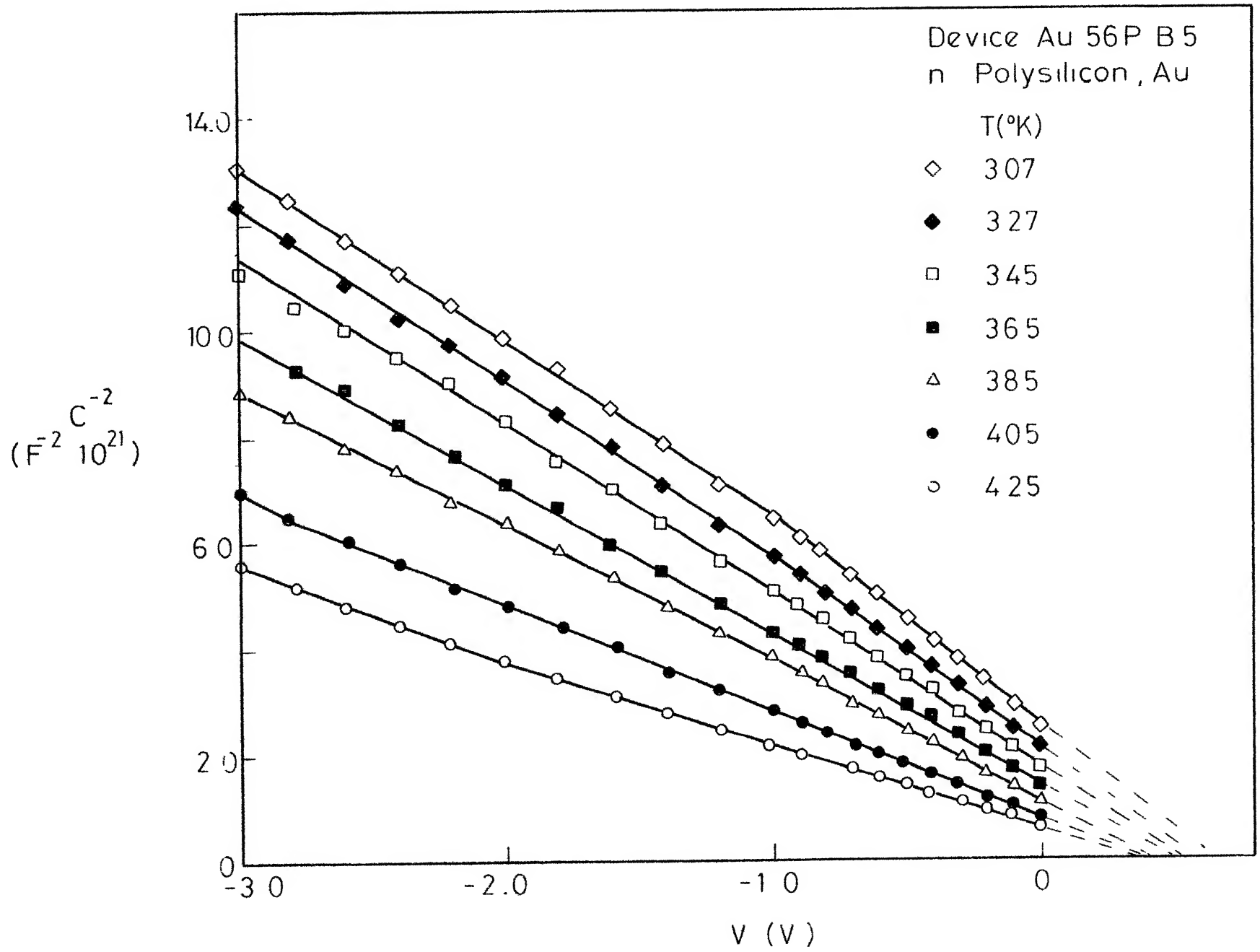
Device Au 56P B5
n Polysilicon, Au
T(°K)
307
327
345
365
385
405
425
14.0
10.0
6.0
2.0
0
-3.0
-2.0
-1.0
0
C^-2 (F^-2 10^21)
V (V)

Fig 4.16

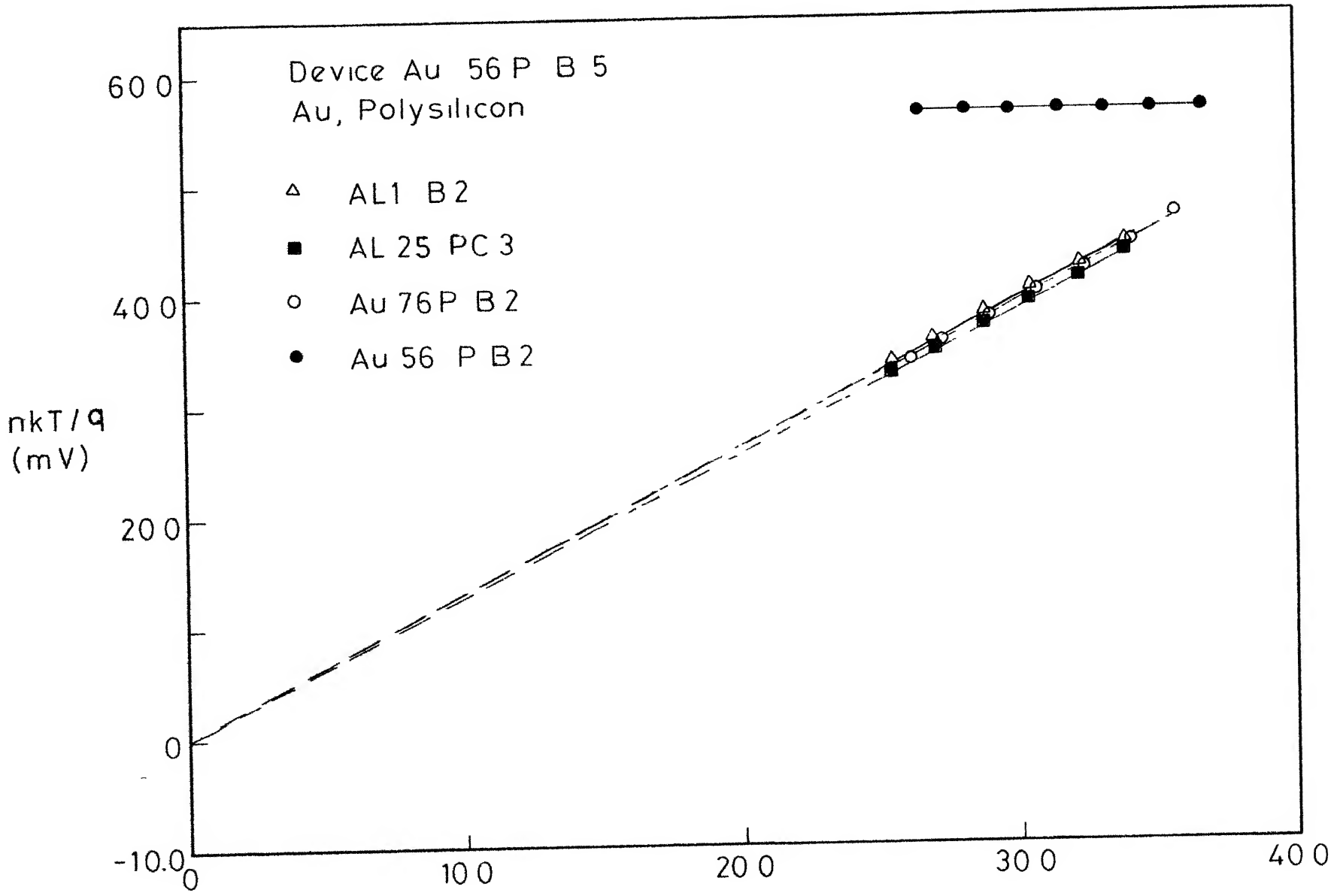
Device Au 56 P B 5
Au, Polysilicon
AL1 B2
AL 25 PC 3
Au 76P B2
Au 56 P B2
nkT/q
(mV)
60 0
40 0
20 0
0
-10.0
0
10 0
20 0
30 0
40 0
kT/q (mV)

Fig 4 17

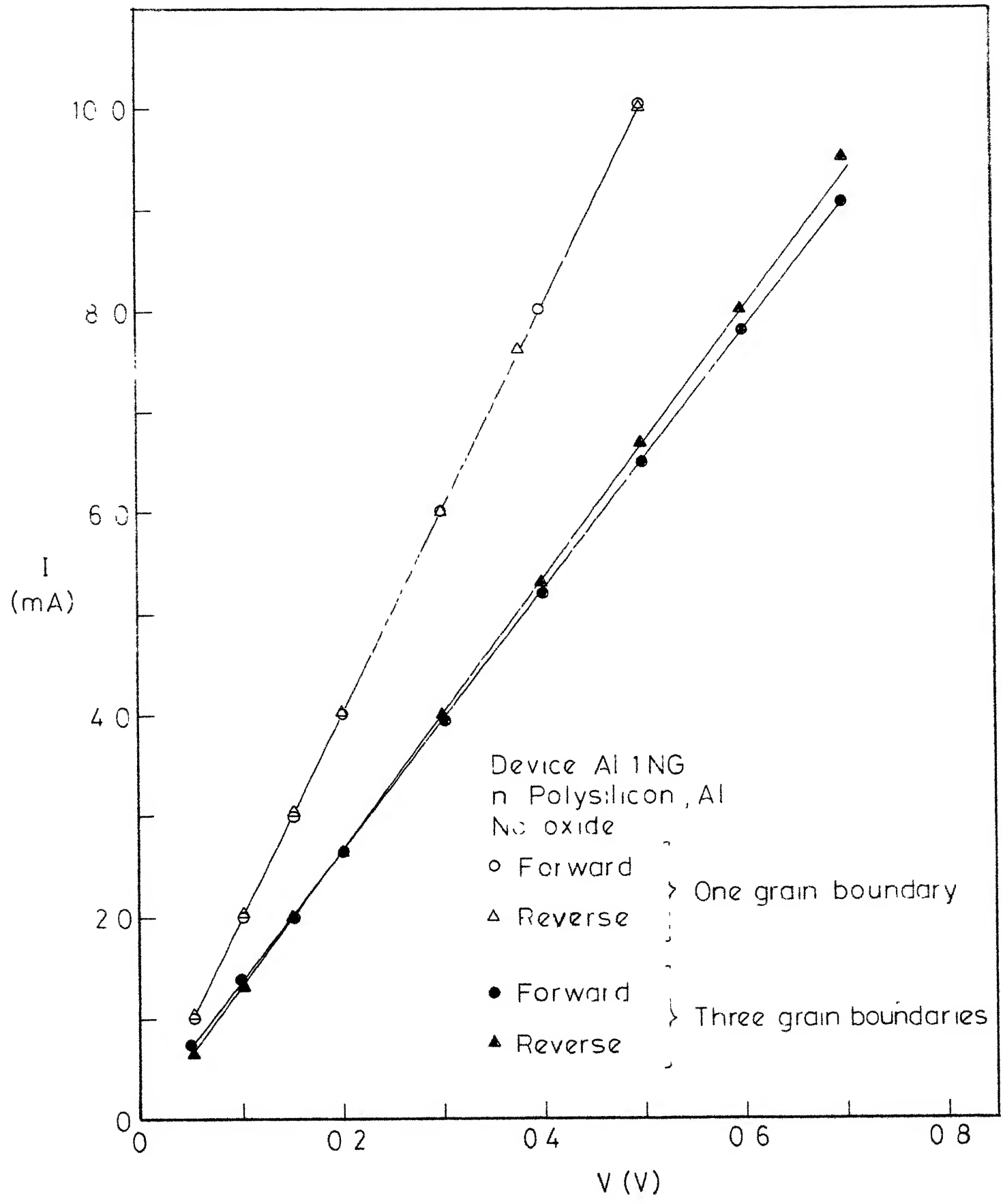
10 0
8 0
6 0
4 0
2 0
0
I
(mA)
0
0 2
0 4
0 6
0 8
V (V)
Device Al 1NG
n Polysilicon , Al
No oxide
o Forward
Δ Reverse
One grain boundary
● Forward
▲ Reverse
Three grain boundaries

Fig 4.18

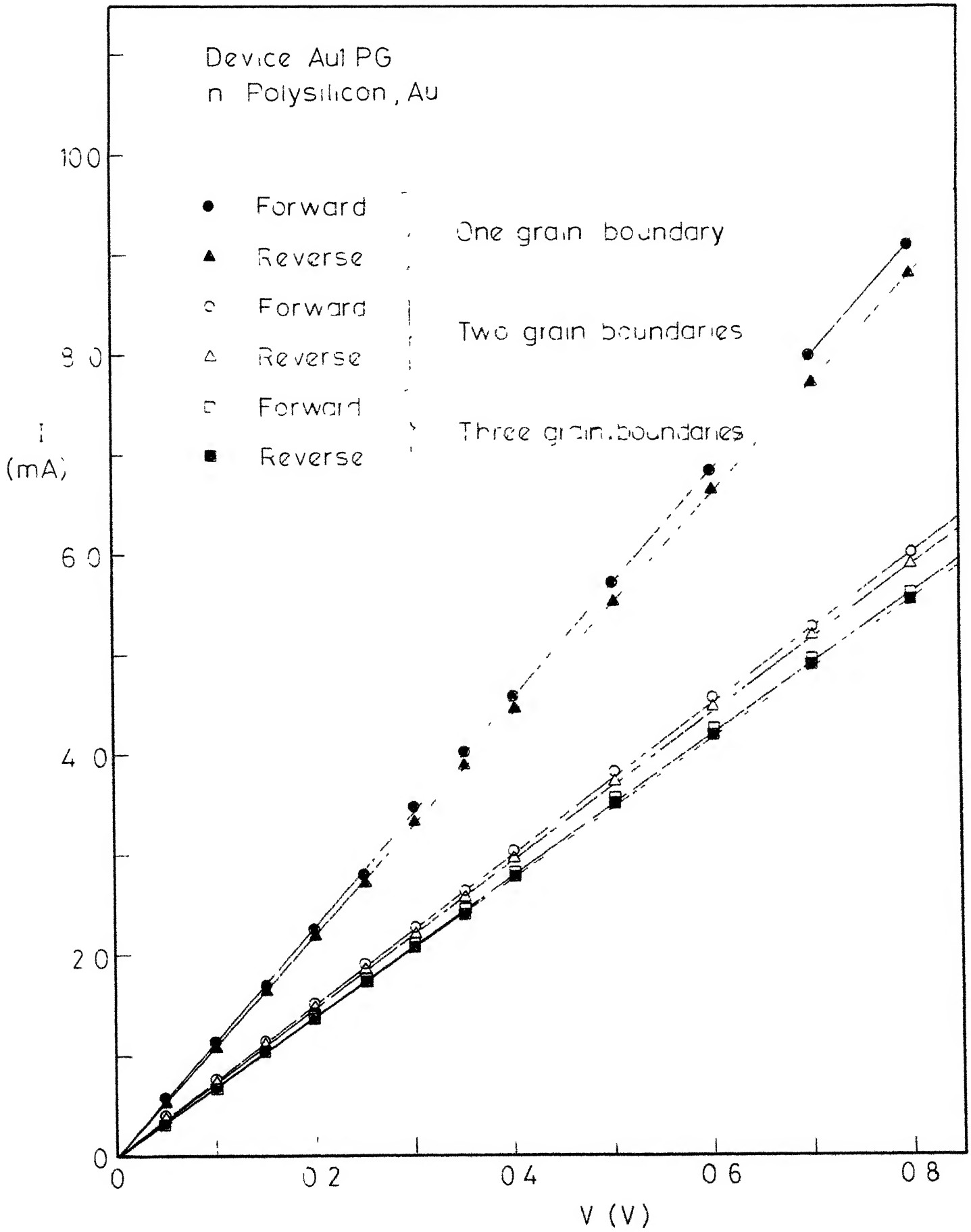
Device Au1 PG
n Polysilicon, Au
Forward
Reverse
Forward
Reverse
Forward
Reverse
One grain boundary
Two grain boundaries
Three grain boundaries
I
(mA)
100
80
60
40
20
0
0
02
04
06
08
V (V)

Fig 4 19

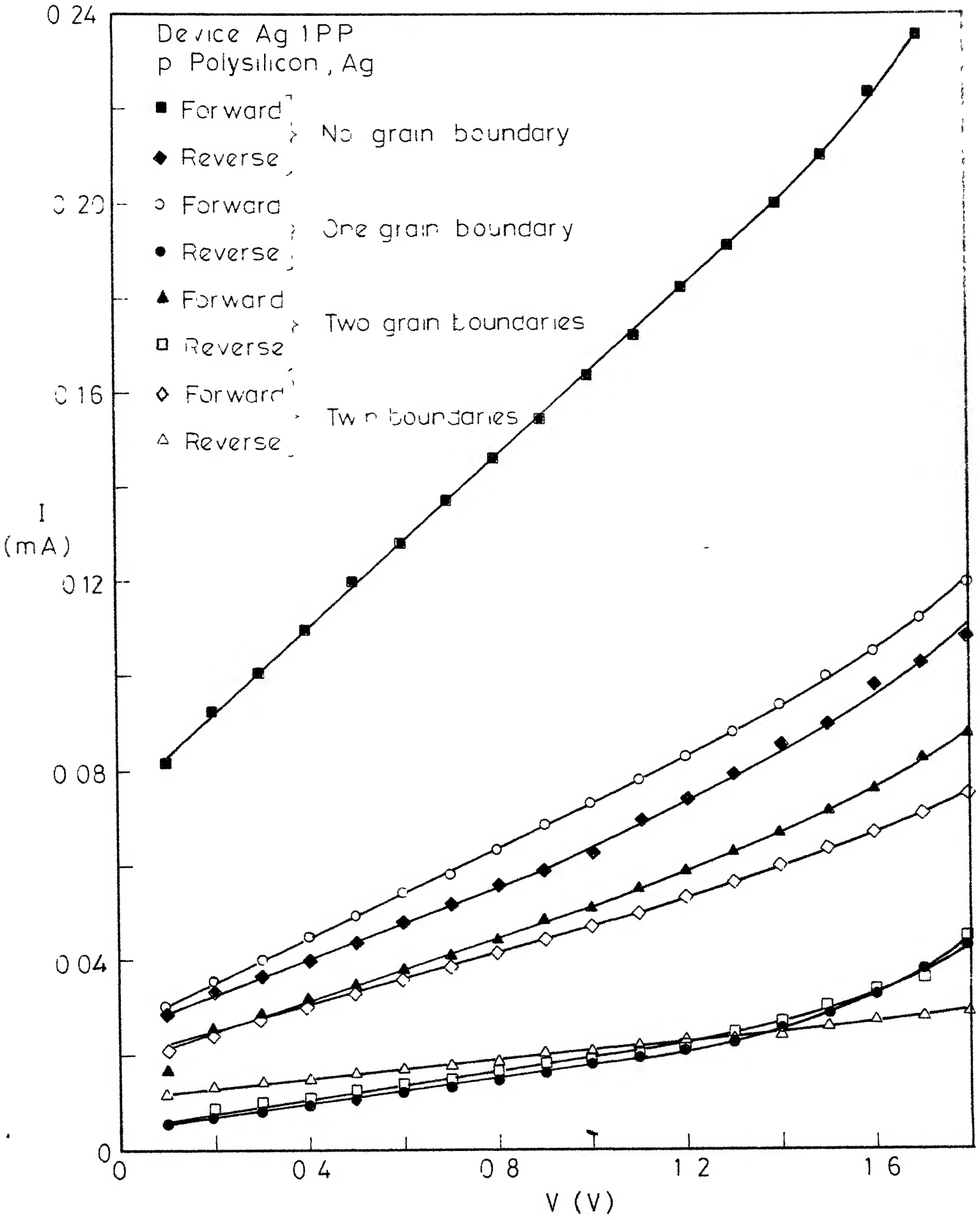
Device Ag 1PP
p Polysilicon , Ag
Forward
Reverse
No grain boundary
Forward
Reverse
One grain boundary
Forward
Reverse
Two grain boundaries
Forward
Reverse
Two boundaries
I
(mA)
0 24
0 20
0 16
0 12
0 08
0 04
0
0
0 4
0 8
1 2
1 6
V (V)

Fig 4 20

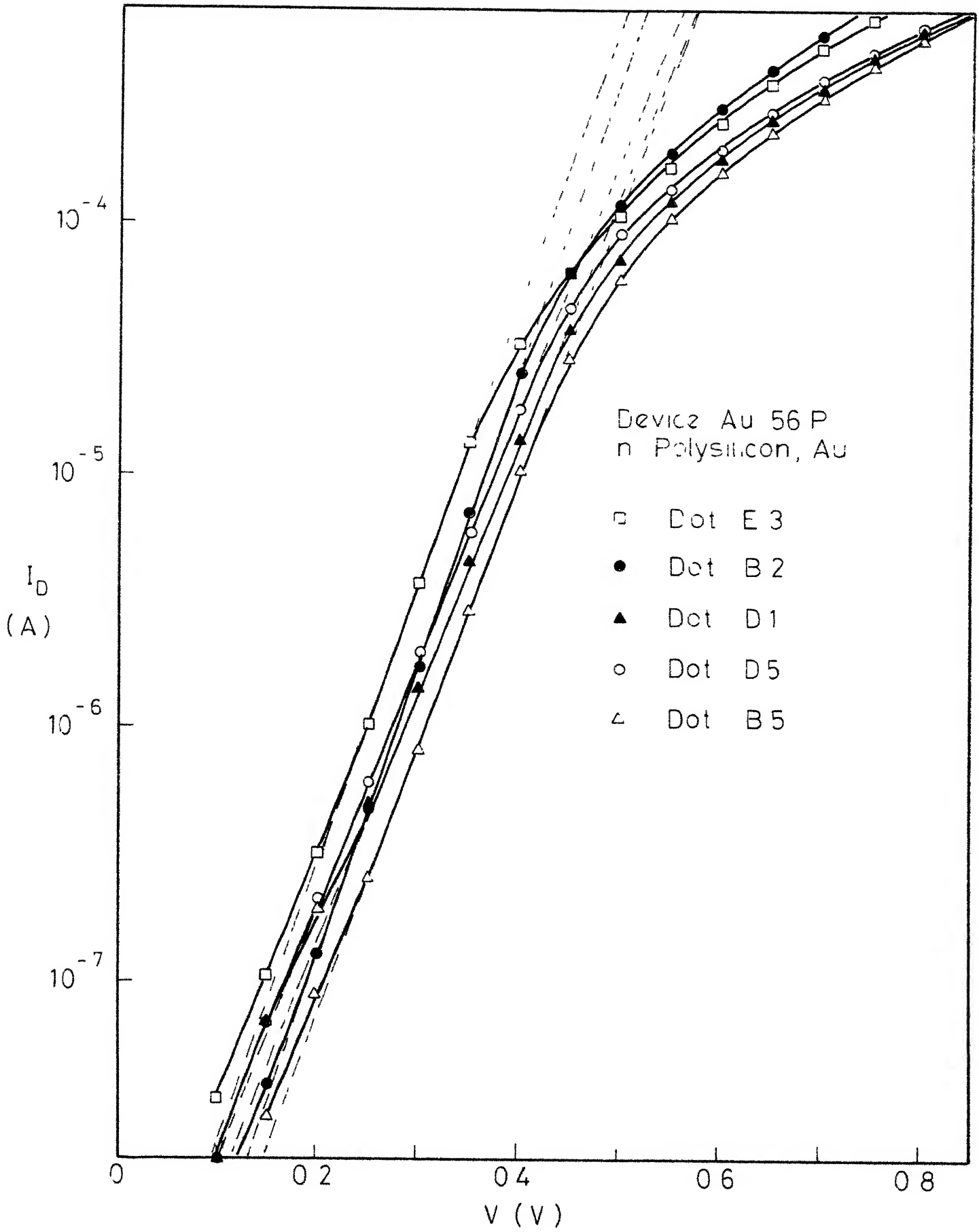
Device Au 56 P
n Polysilicon, Au
Dot E 3
Dot B 2
Dot D 1
Dot D 5
Dot B 5
10^{-4}
10^{-5}
10^{-6}
10^{-7}
I_D
(A)
0
0 2
0 4
0 6
0 8
V (V)

Fig 4 21

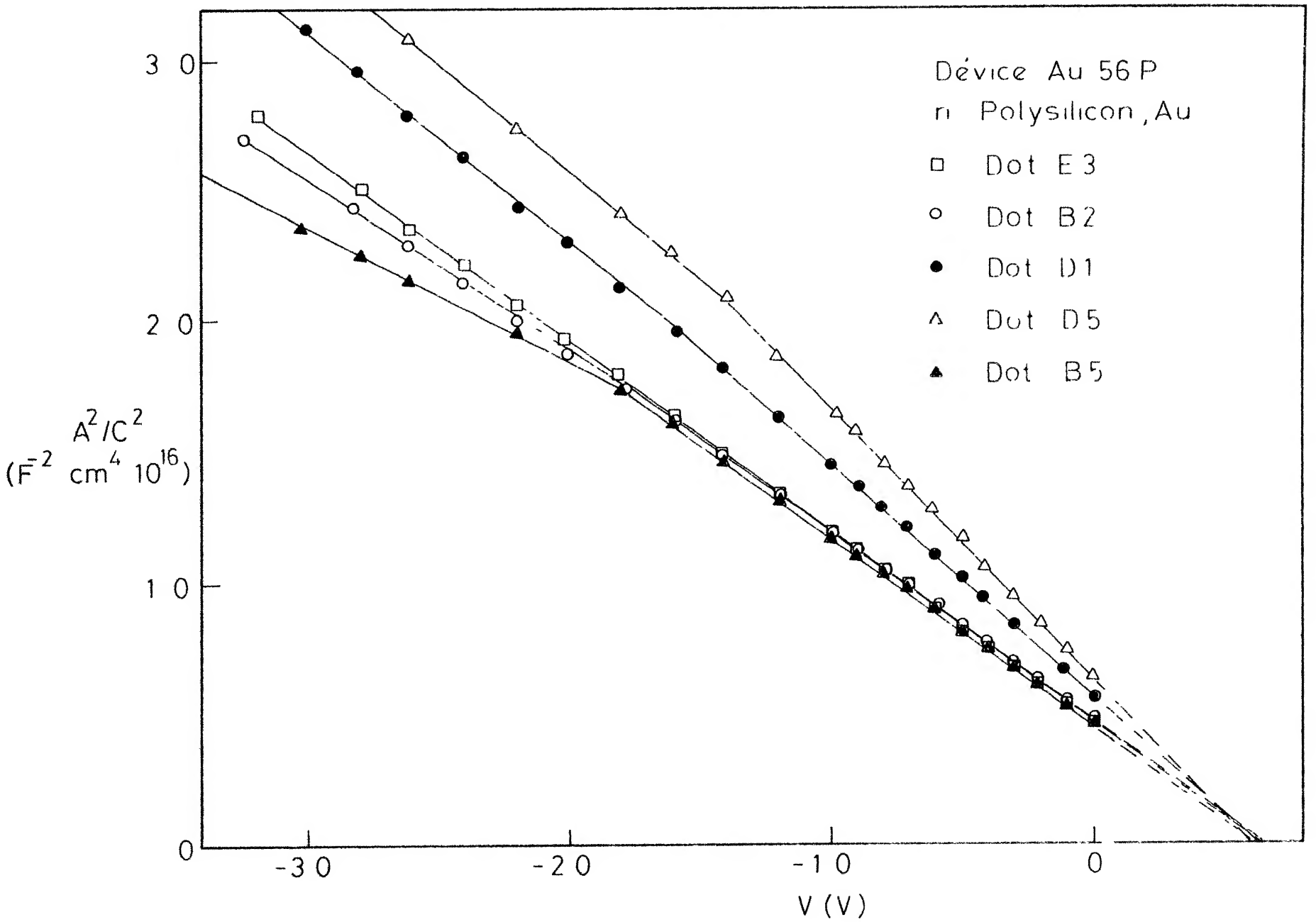
Dévice Au 56 P
n Polysilicon, Au
Dot E 3
Dot B 2
Dot D 1
Dot D 5
Dot B 5
3 0
2 0
1 0
0
A²/C²
(F⁻² cm⁴ 10¹⁶)
-30
-20
-10
0
V (V)

Fig 4 22

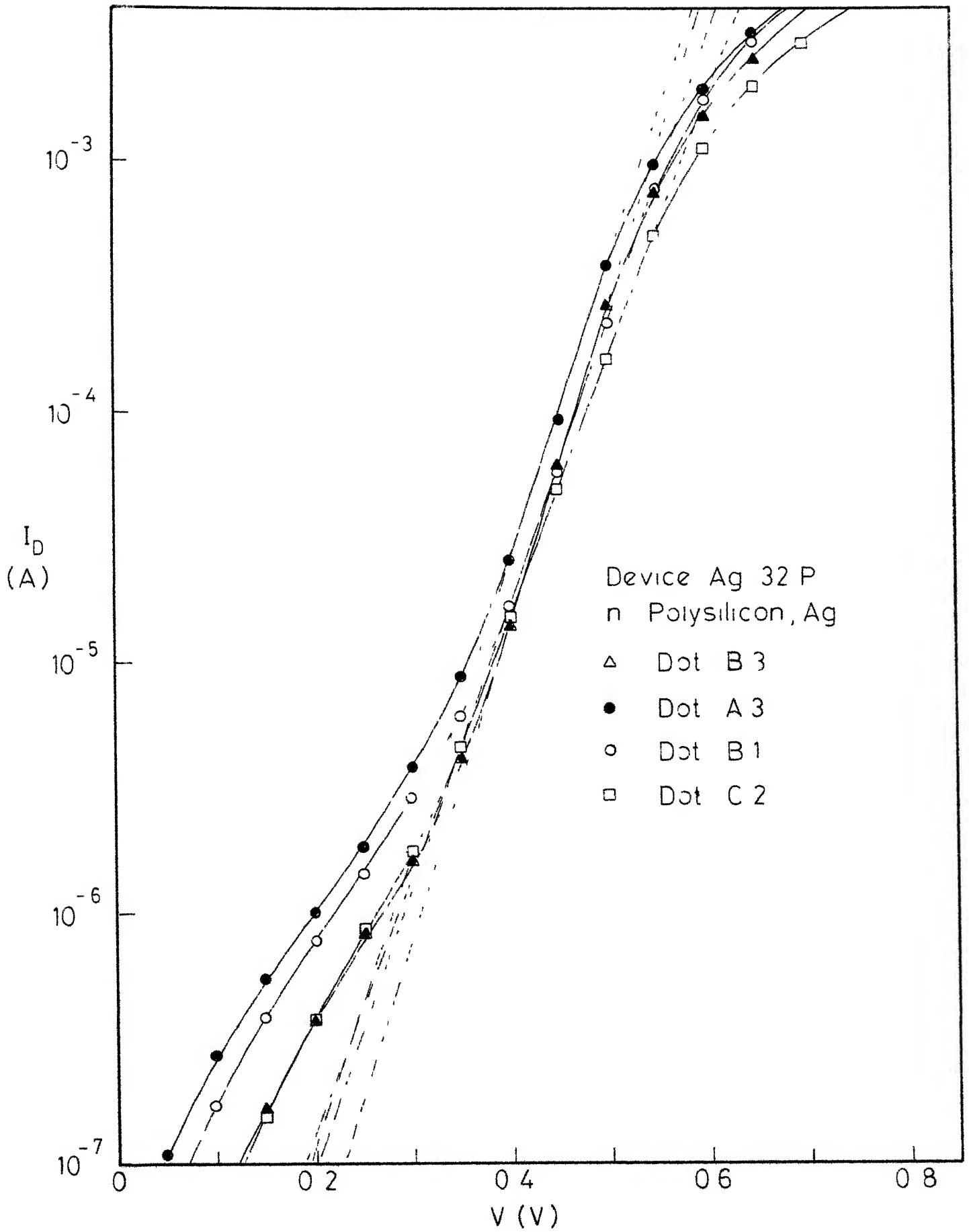
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
I_D
(A)
0
0 2
0 4
0 6
0 8
V (V)
Device Ag 32 P
n Polysilicon, Ag
Dot B 3
Dot A 3
Dot B 1
Dot C 2

Fig 4 23

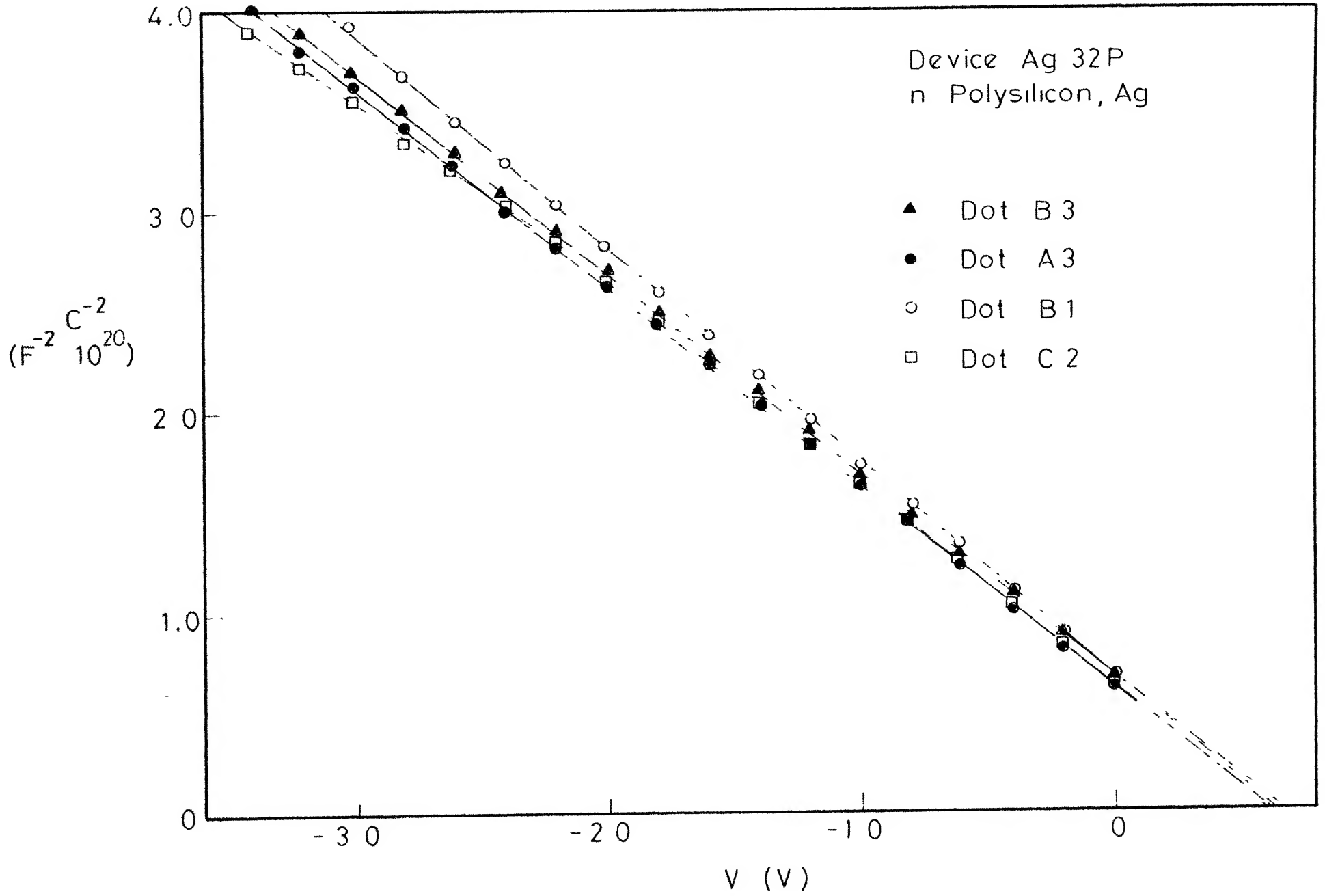
Device Ag 32P
n Polysilicon, Ag
Dot B 3
Dot A 3
Dot B 1
Dot C 2
4.0
3 0
2 0
1.0
0
-3 0
-2 0
-1 0
0
C^-2 (F^-2 10^20)
V (V)

Fig 4 24